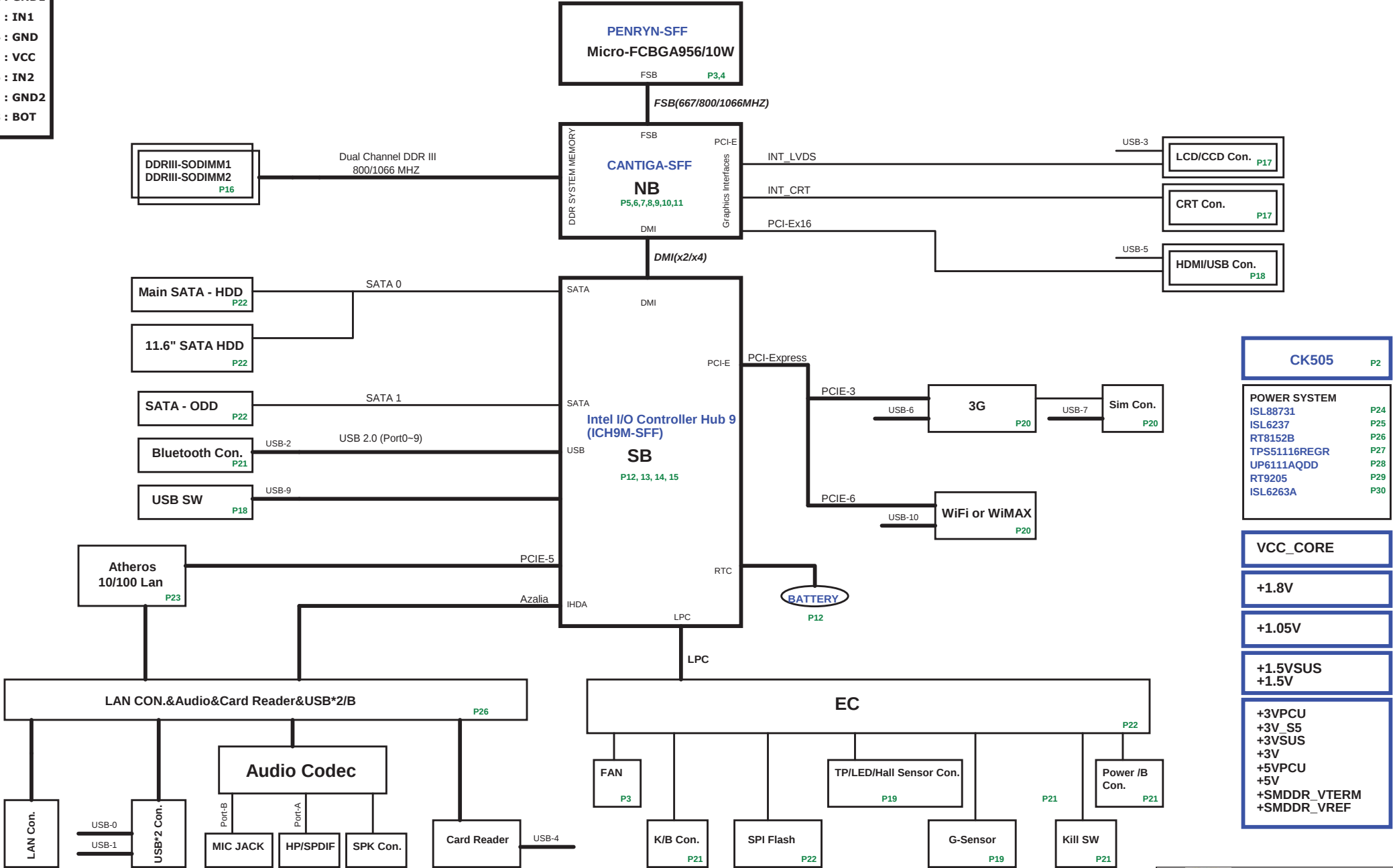


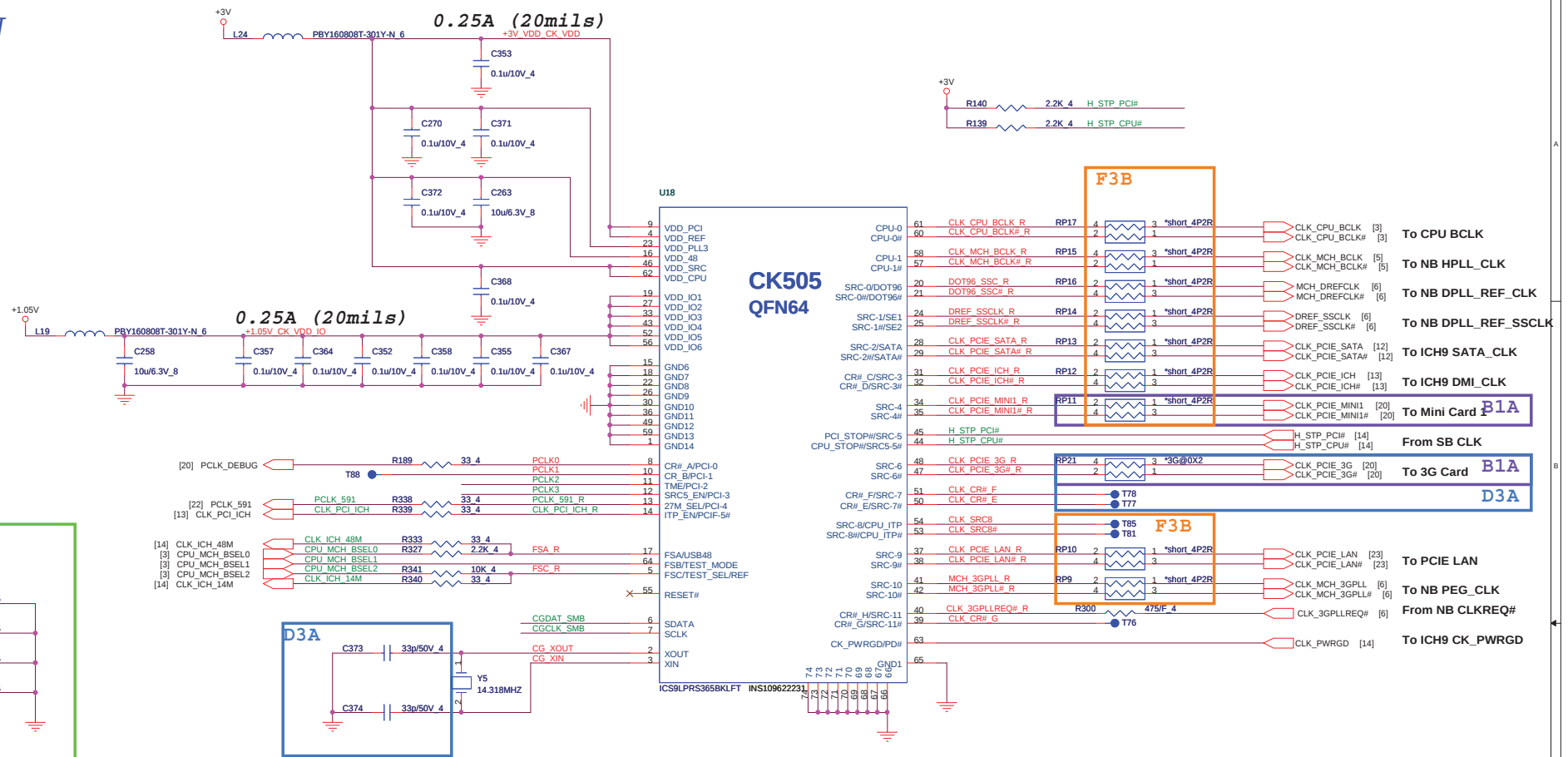
PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : GND1
- LAYER 3 : IN1
- LAYER 4 : GND
- LAYER 5 : VCC
- LAYER 6 : IN2
- LAYER 7 : GND2
- LAYER 8 : BOT

BU3 Block Diagram

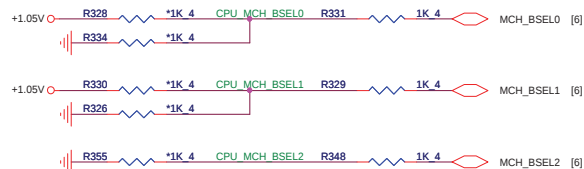


CLOCK GEN



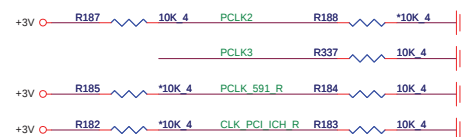
BSEL Frequency Select Table

FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSD	100	33

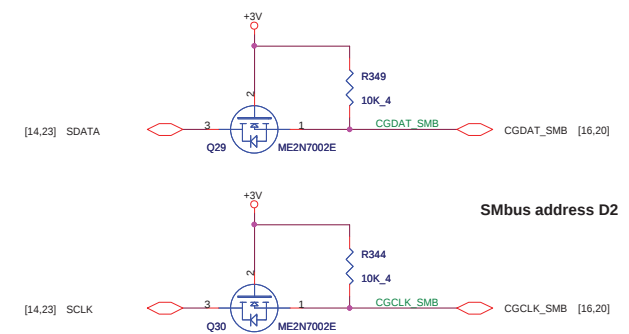


Clock Gen Strap

	SL98SP513	PULL HIGH	PULL DOWN
PIN11	PCI2/TWE	NO OVERCLOCKING (default)	NORMAL RUN
PIN12	PCI-3	PIN44/45 IS SRC5	PIN44/45 IS PCI_STOP/CPU_STOP (default)
PIN13	PCI-4/27M_SEL	PIN 24/25 IS 27MHz	PIN 21/20 IS SRC/DOT (default)
PIN14	PCIP-5/ITP_EN	PIN 53/54 IS CPUITP	PIN 53/54 IS SRC (default)



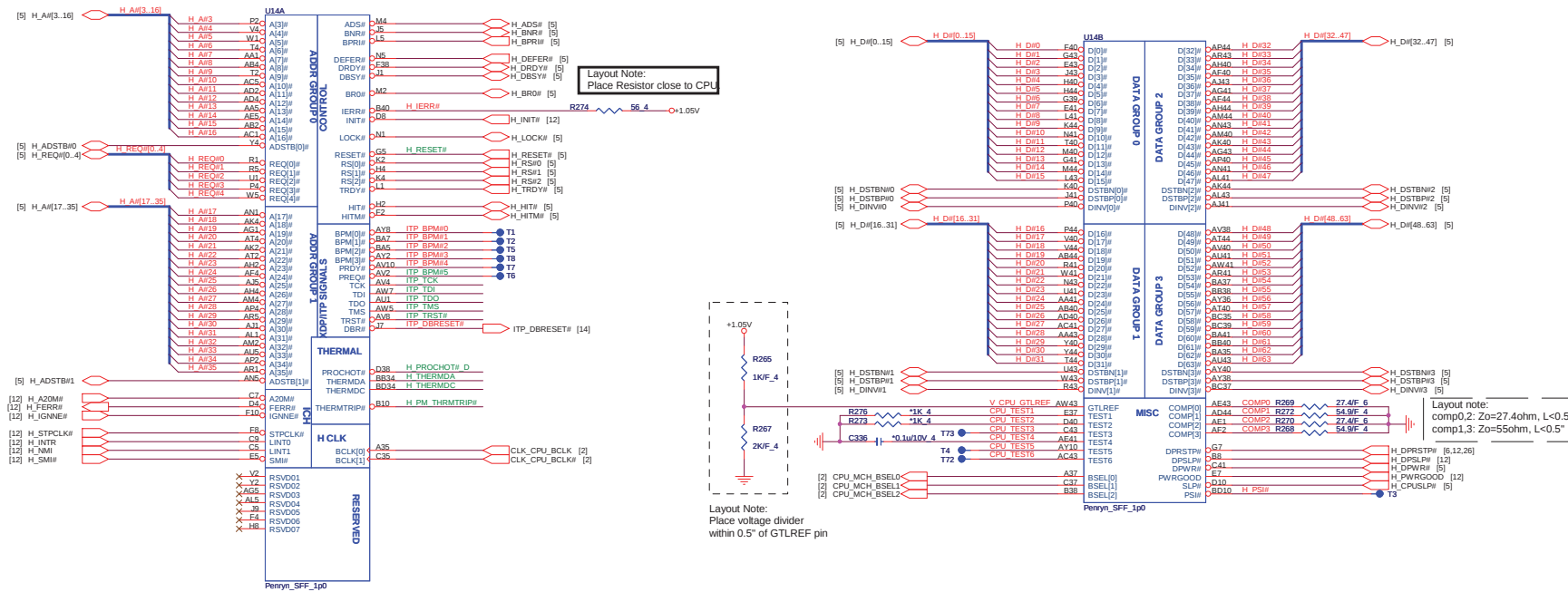
Clock Gen I2C



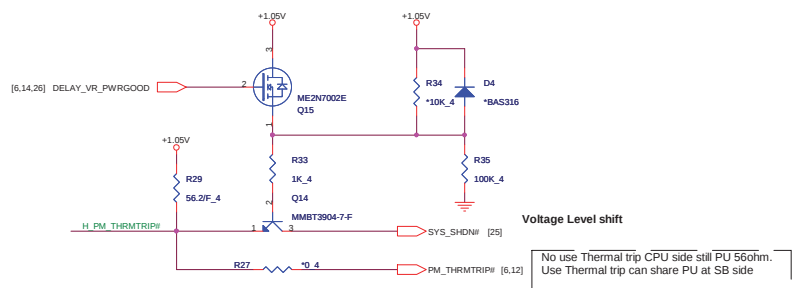
PROJECT : BU3
Quanta Computer Inc.

Size Custom	Document Number CLOCK GEN_9LPRS365BKLFT	Rev D3B
Date: Monday, August 10, 2009	Sheet 2 of 34	

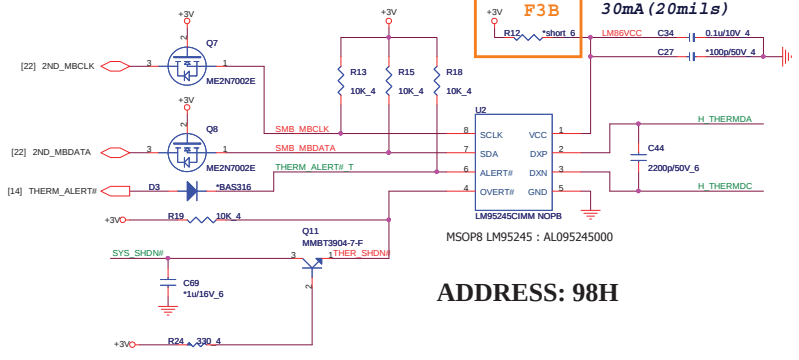
CPU



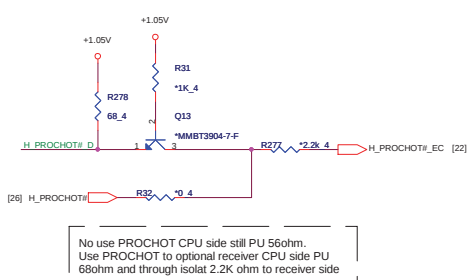
Thermal Trip



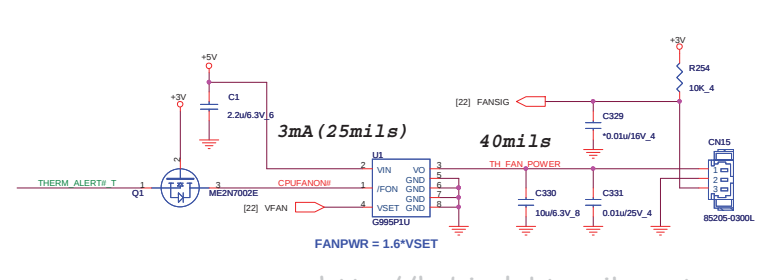
CPU Thermal Monitor



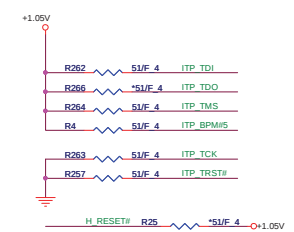
Processor Hot



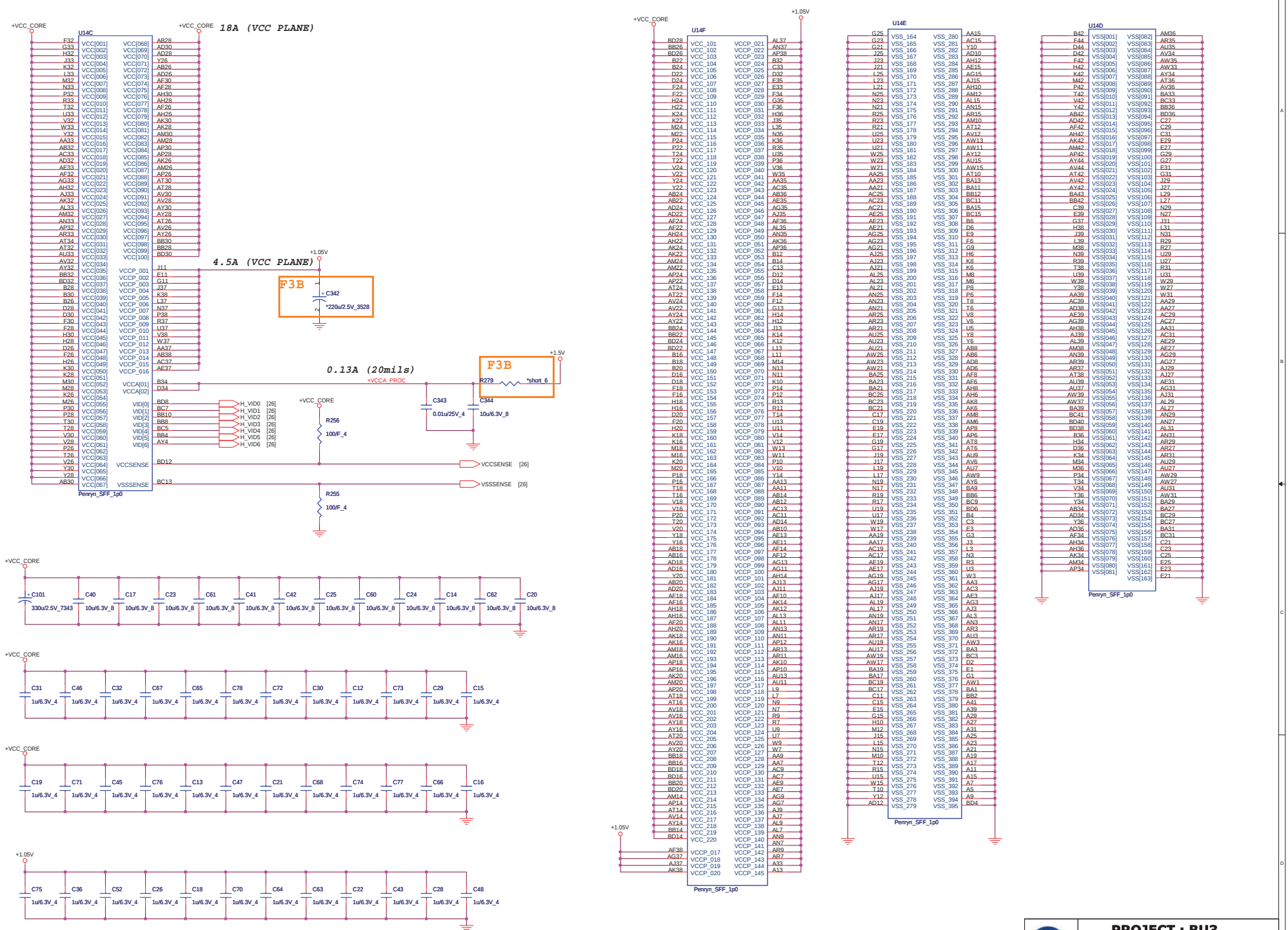
CPU FAN CTRL

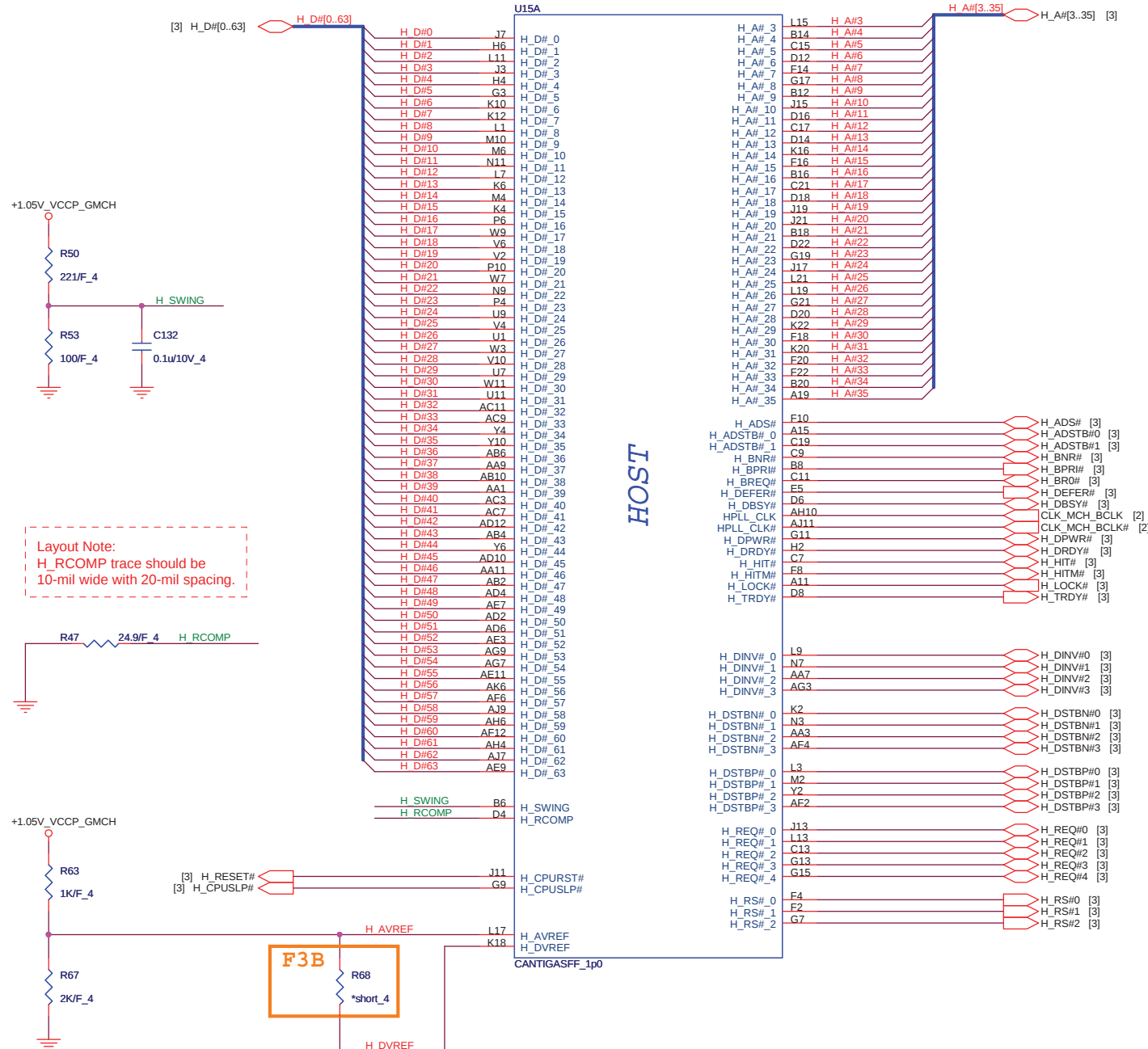


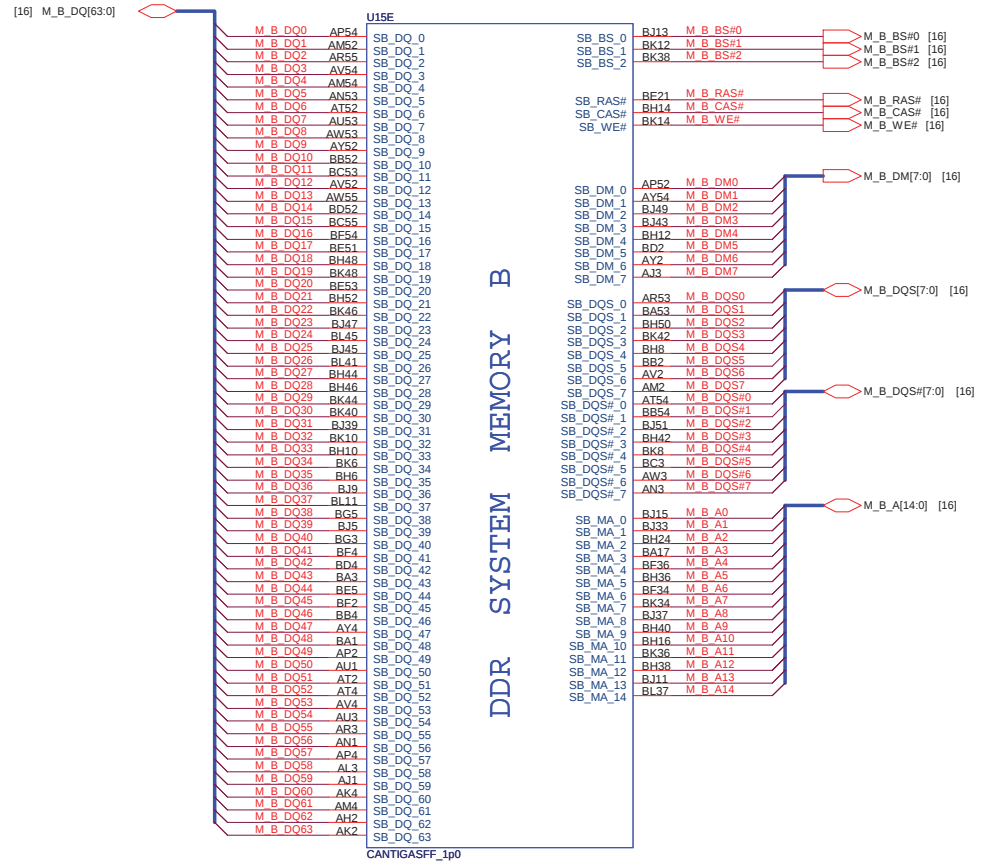
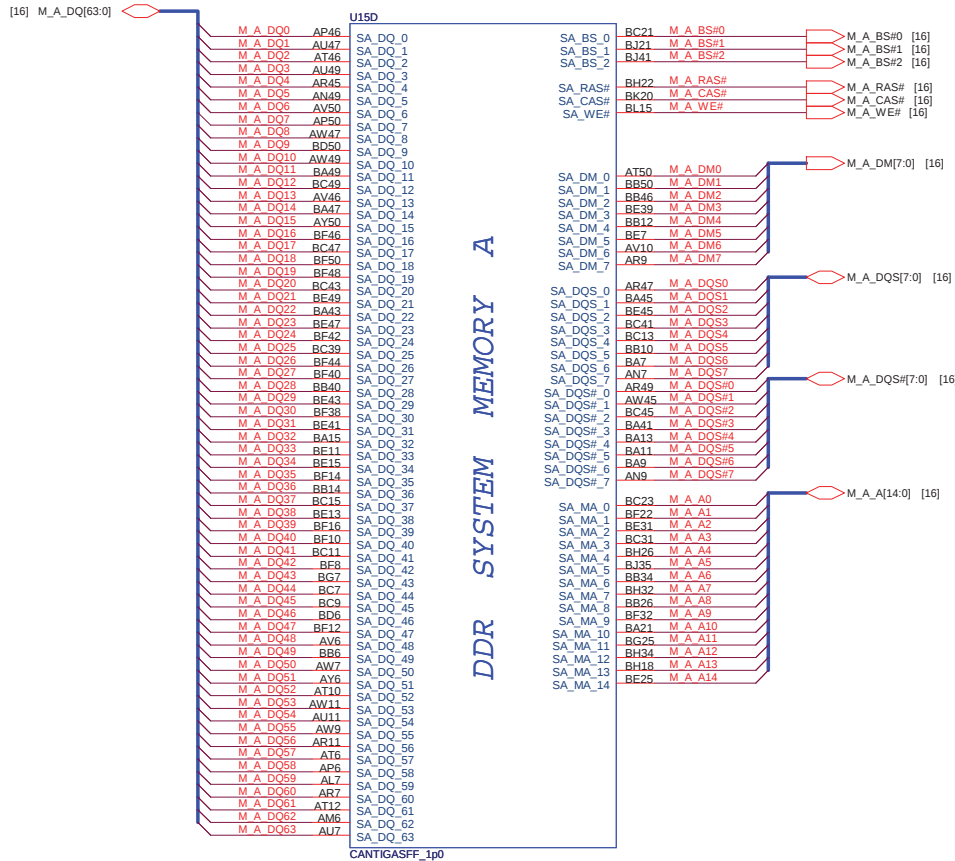
XDP



Layout Note:
Place Resistor close to CPU
with Stub length <200mils.



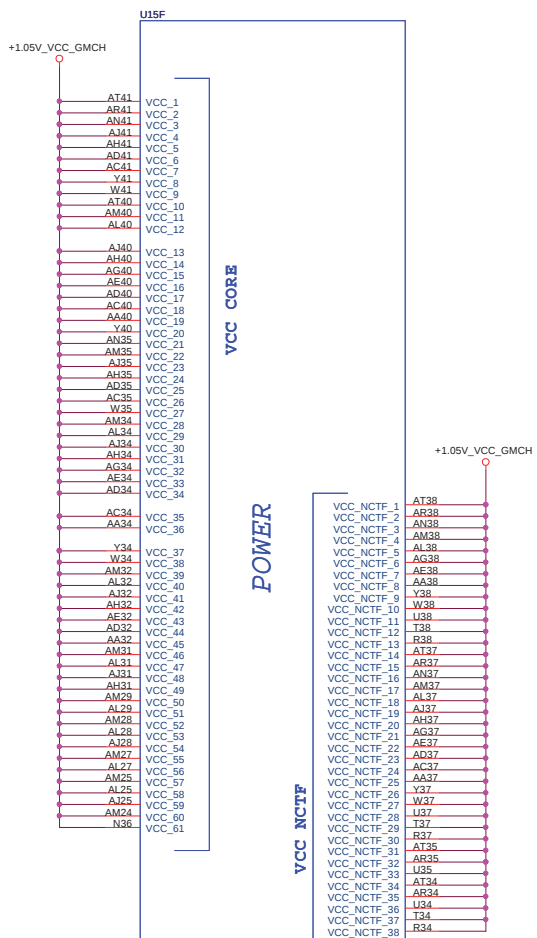




DDR SYSTEM MEMORY A

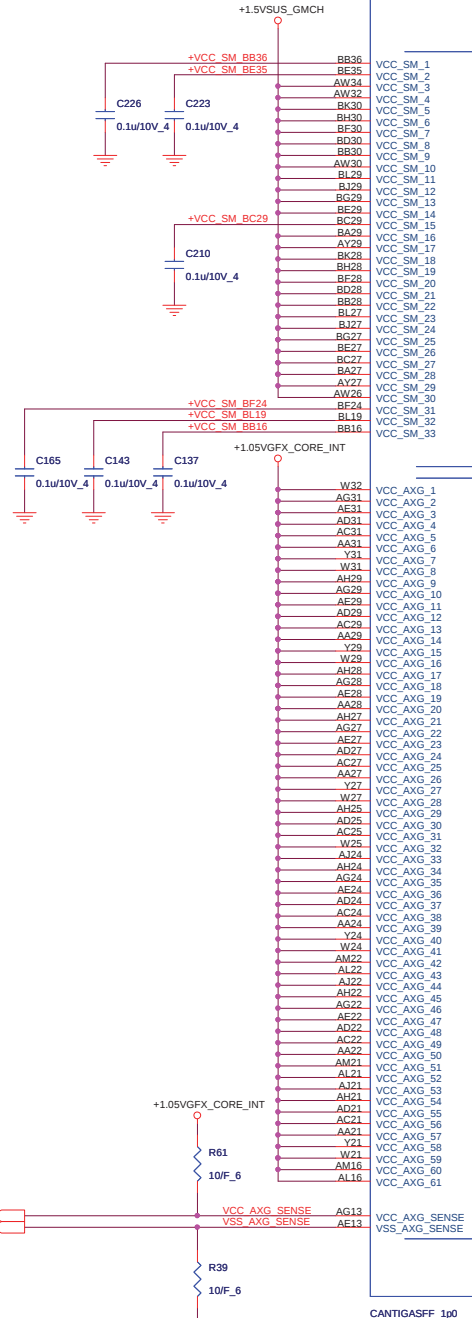
DDR SYSTEM MEMORY B

lvcc internal VGA 2.2A
(Shape or 120mils)



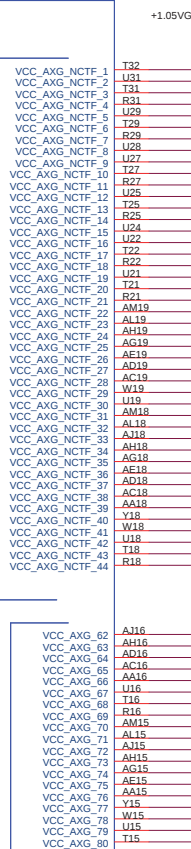
[30] VCC_AGX_SENSE
[30] VSS_AGX_SENSE

DDR3-800 3.1625A
DDR3-1066 4.14A
(Shape or 200mils)

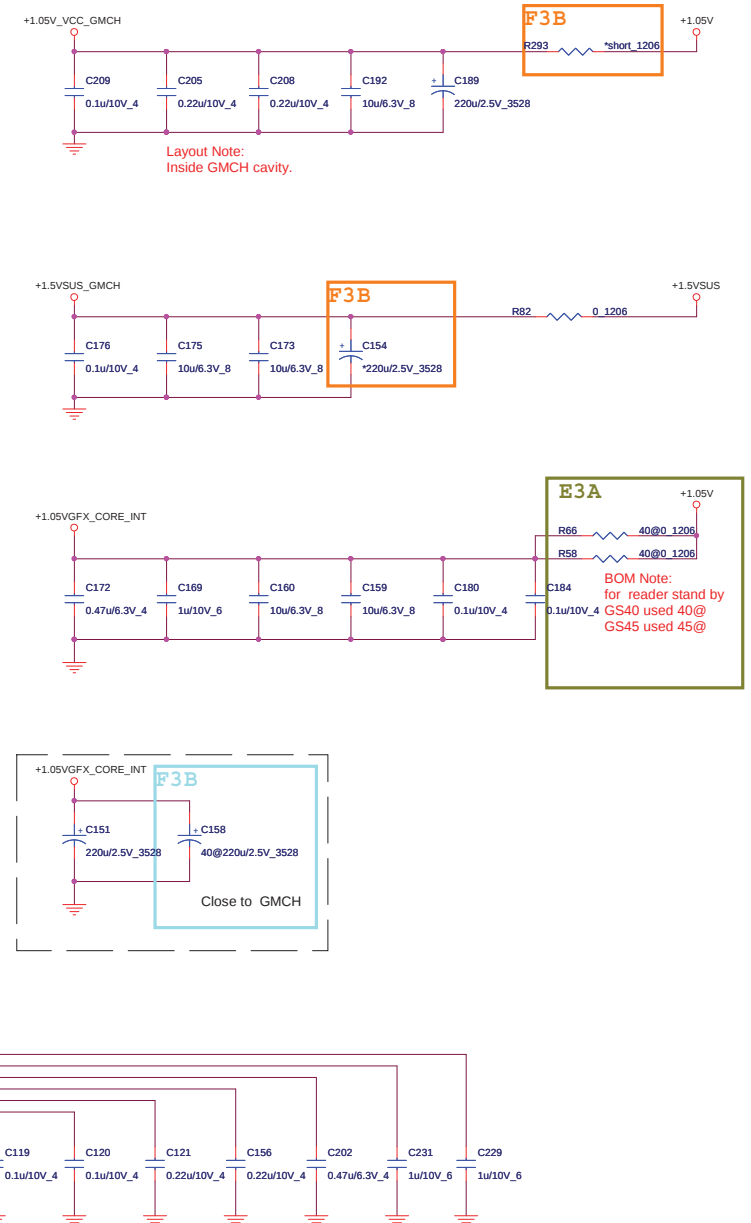


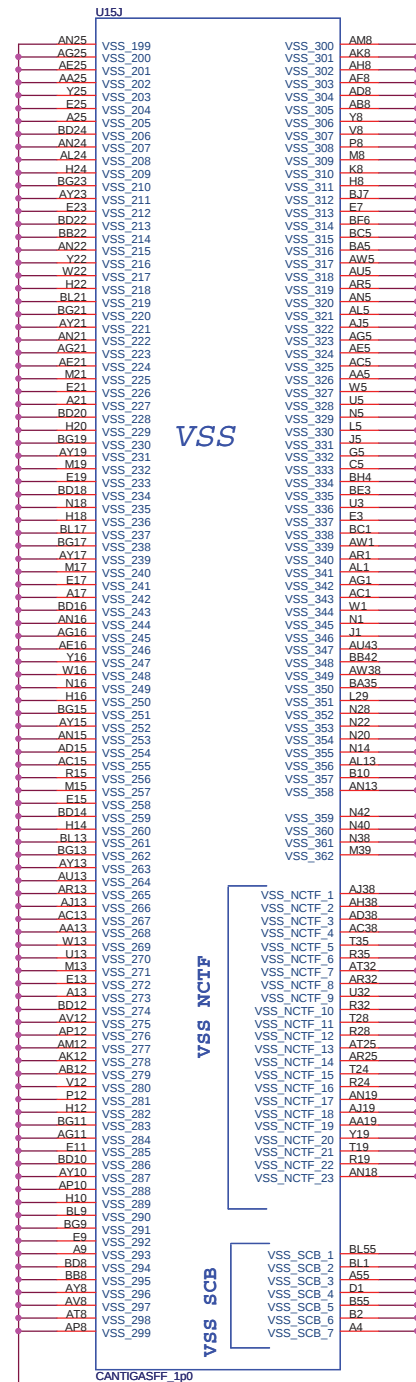
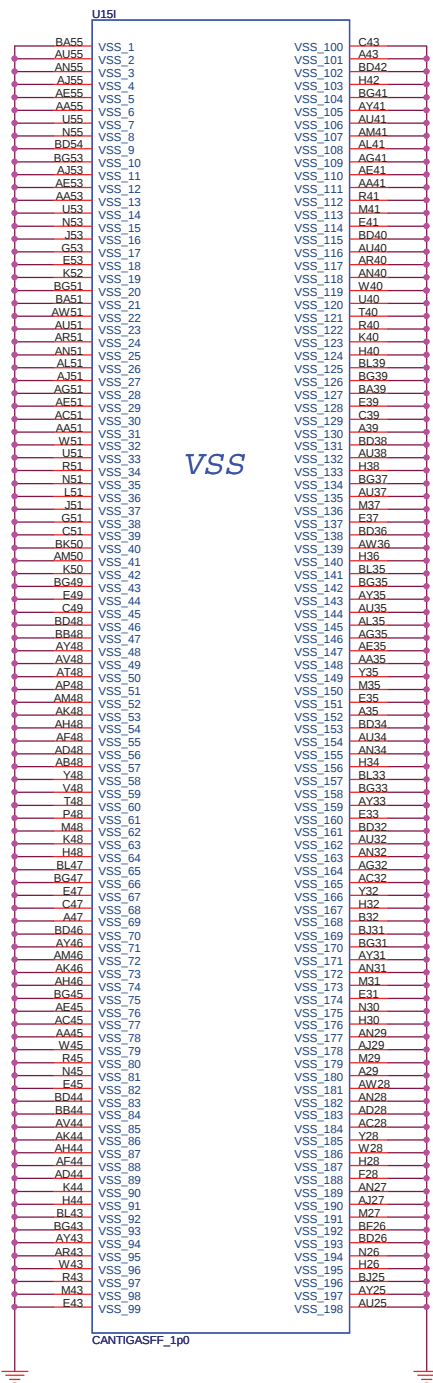
UMA: Places R721, R726 to 10 ohm.

UMA 9.6A
(Plane or shape)



VCC SM I/F





PROJECT : BU3
Quanta Computer Inc.

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North Bridge Strap Pin Configuration Table

(See DG 2.0 P306 Table 187)
(See NB EDS 1.0 P187 Table 74)

Pin Name	Strap description	Configuration	PU<4.02K> PD <2.21K>	Note
CFG[2:0]	FSB Frequency Select	[000]= FSB 1066MHz [010] = FSB 800MHz [011] = FSB 667MHz	See Page 2 FSB selection table	
CFG[4:3]	Reserved			
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)	[6] MCH_CFG5	
CFG6	iTPM Host Interface	0 = iTPM Host Interface is enabled 1 = iTPM Host Interface is disabled(Default)	[6] MCH_CFG6	
CFG7	ME TLS Confidentiality	0 = AMT Firmware will use TLS cipher suite with no confidentiality 1 = AMT Firmware will use TLS cipher suite with confidentiality(Default)	[6] MCH_CFG7	
CFG8	Reserved			
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)	[6] MCH_CFG9	
CFG10	PCIe Loopback enable	0 = Enabled 1 = Disabled (Default)	[6] MCH_CFG10	
CFG11	Reserved			
CFG12	ALLZ	0 = ALLZ mode enable 1 = disable(Default)	[6] MCH_CFG12	
CFG13	XOR	0 = XOR mode enable 1 = disable(Default)	[6] MCH_CFG13	
CFG[15:14]	Reserved			
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)	[6] MCH_CFG16	
CFG[18:17]	Reserved			
CFG19	DMI Lane Reversal	0 = Normal (Default) 1 = Lanes Reversed	[6] MCH_CFG19	
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIE	0 = Only Digital Display port (SDVO/DP/iHDMI) or PCIE is operational (Default) 1 = Digital Display port (SDVO/DP/iHDMI) and PCIE are operating simultaneously via PEG port	[6] MCH_CFG20	
SDVO_CTRLDATA	SDVO Present	0 = No SDVO/HDMI/DP Device Present(Default) 1 = SDVO/HDMI/DP Device present	Strap on P18 SDVO_CTRLDATA	
L_DDC_DATA	Local Flat Panel(LFP) Present	0 = LFP Disable(Default) 1 = LFP Card Present;PCIE disable	Strap on P17 INT_LVDS_EDIDDATA	
DDPC_CTRLDATA	Digital Display Present	0 = Digital display(HDMI/DP) device absent(Default) 1 = Digital display(HDMI/DP) device present	[6] DDPC_CTRLDATA	

[6] DDPC_CTRLCLK

Enable iTPM Table

PAGE	Net Name	PU & PD	NOTE
11	MCH_CFG_6	PD 10K to GND	NB Strap pin
13	SPI_MOSI	PU 20K to +3V_S5	SB Strap pin
14	CLGP105	PU 10K to +3V_S5	SB Strap pin



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Size

Document Number

Rev

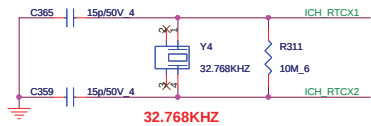
NB (7/7)- STRAP PIN

D38

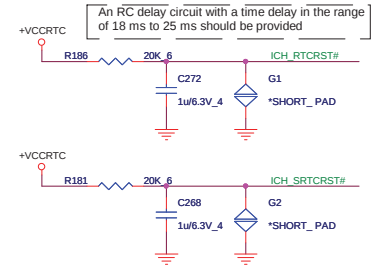
Date: Monday, August 10, 2009

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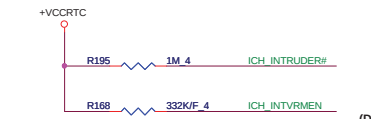
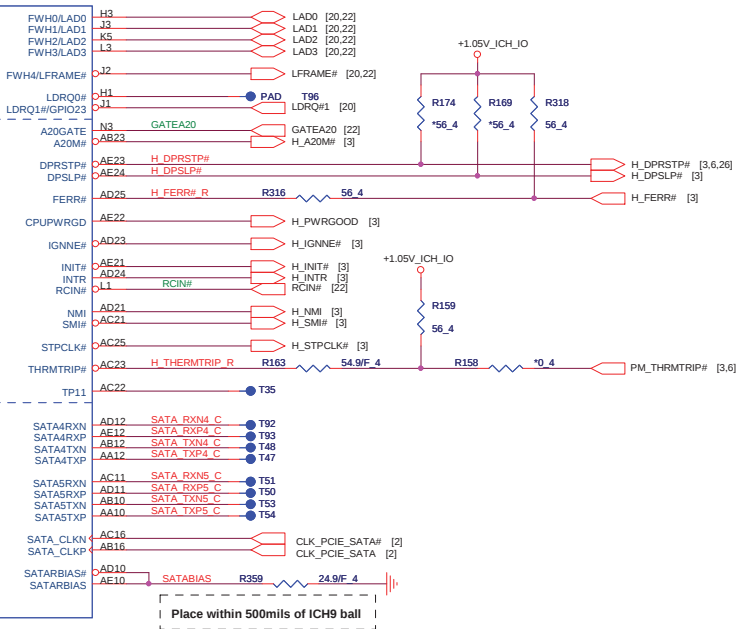
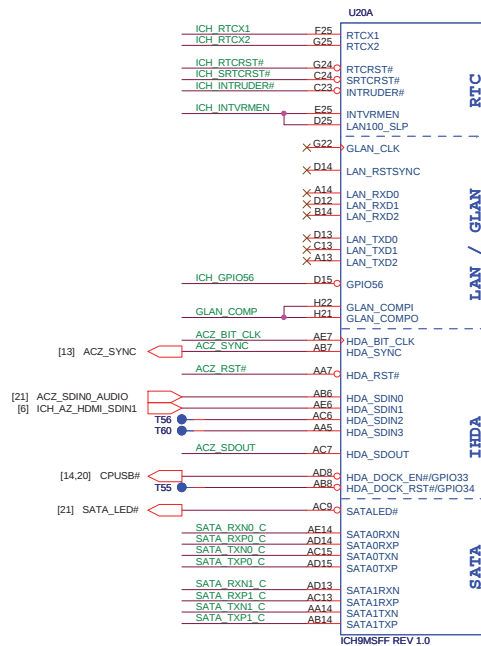
RTC CRYSTAL



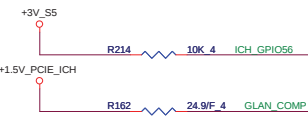
RESET JUMP



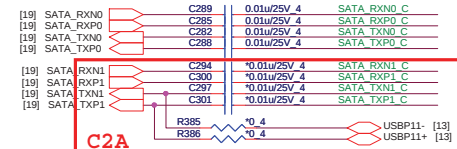
ICH_SATA_LED#	
0	PCIe Lane Reversed
1	PCIe Straight(default)



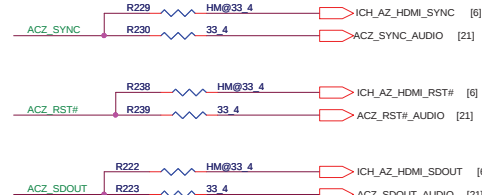
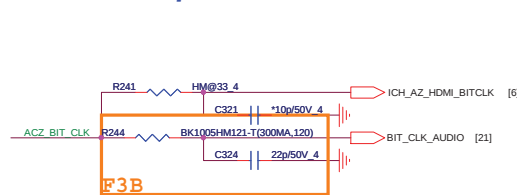
(DG 1.0 Table-292)
Internal vRM enabled for VccSus1_05, VccSus1_5, VccCL1_5, VccLAN1_05 and VccCL1_05.



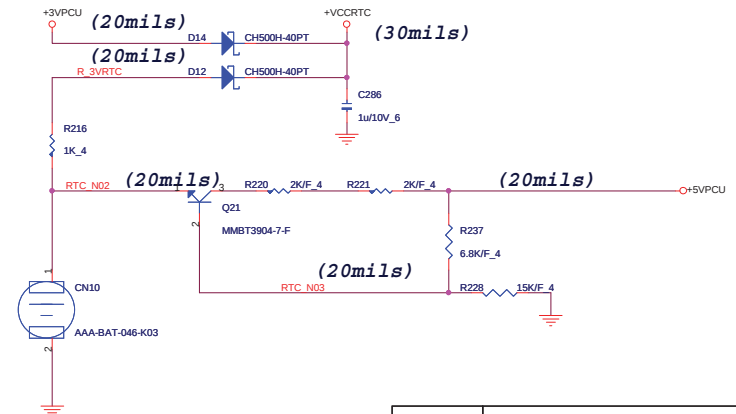
24.9 Ohm pull up to 1.5V for GLAN_COMP is required, no matter intel LAN is used or not.



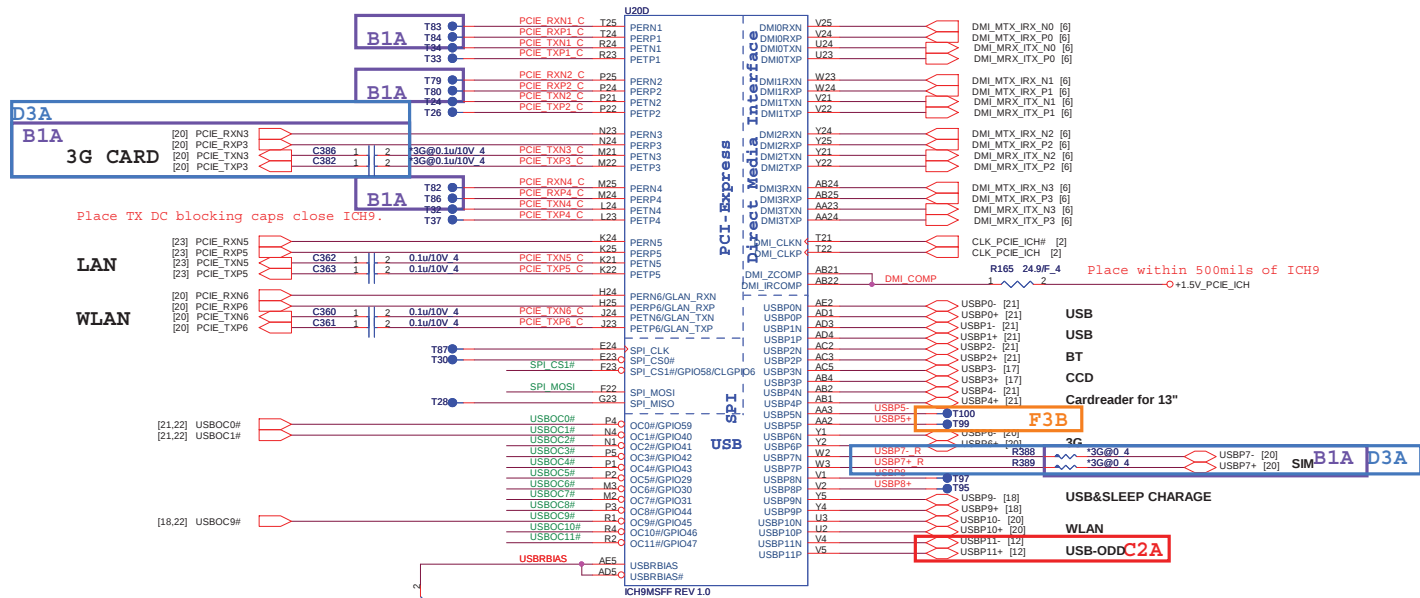
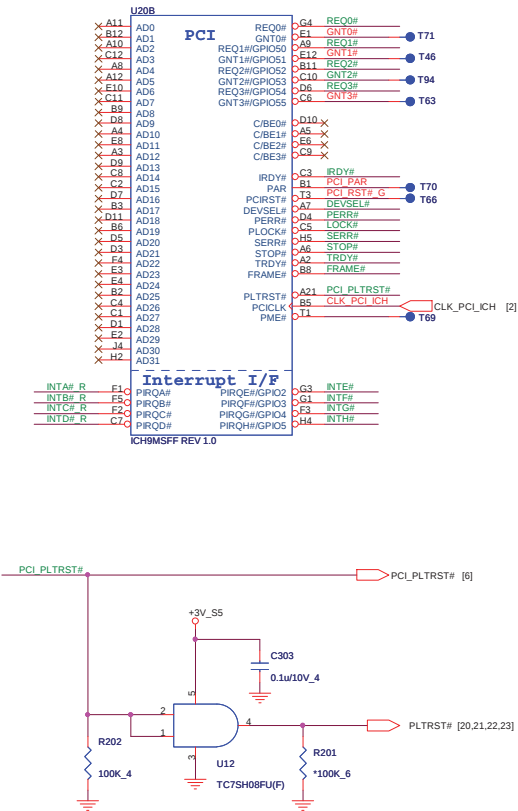
HD Audio Interface



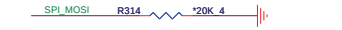
RTC BATTERY



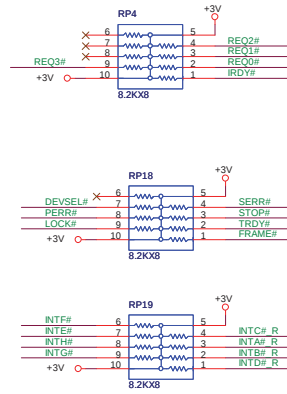
ICH9



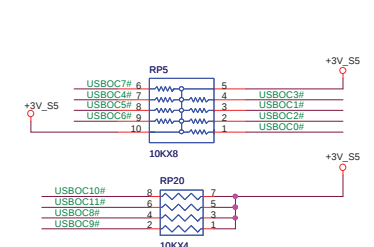
South Bridge Strap Pin (2/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD		
HDA_SYNC	PCI Express Port Config 1 bit 0 (Port 1-4)	PWROK	0 = Default 1 = Setting bit 0			
GNT2# / GPIO53	PCI Express Port Config 2 bit 2 (Port 5-6)	PWROK	0 = Setting bit 2 1 = Default			
GNT1# / GPIO51	ESI Strap(Server Only)	PWROK	0 = DMI for ESI-compatible 1 = Default			
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default			
SPI_MOSI	Integrated TPM Enable	CLPWROK	0 = INT TPM disable(Default) 1 = INT TPM enable			
GNT0#	Boot BIOS Selection 0	PWROK	PCI_GNT#0	SPI_CS#1	Boot Location	
			0	1	SPI(Default)	
SPI_CS1# / GPIO58 / CLGPIO6	Boot BIOS Selection 1	CLPWROK	1	0	PCI	
						

PCI PULL-UP

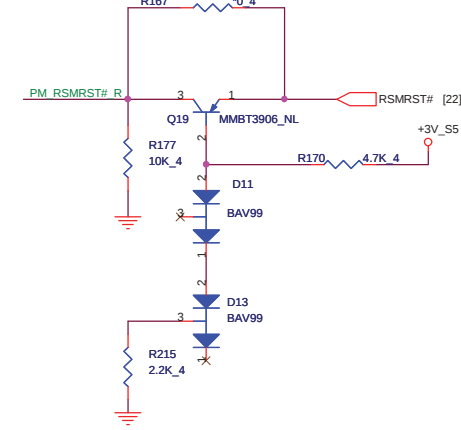
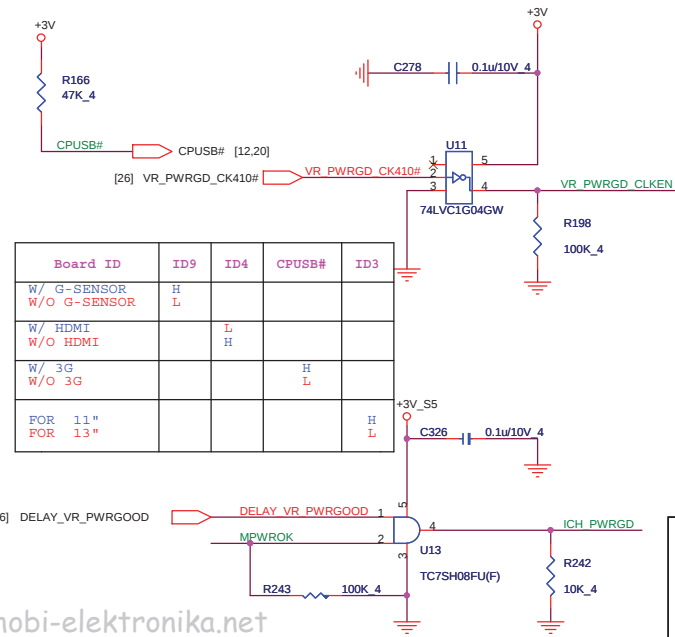
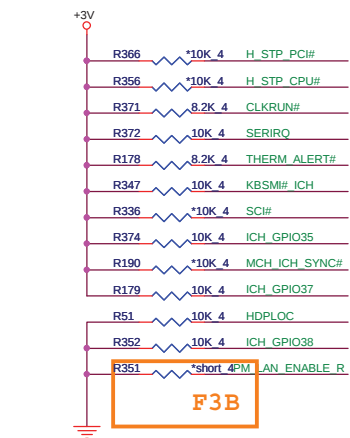
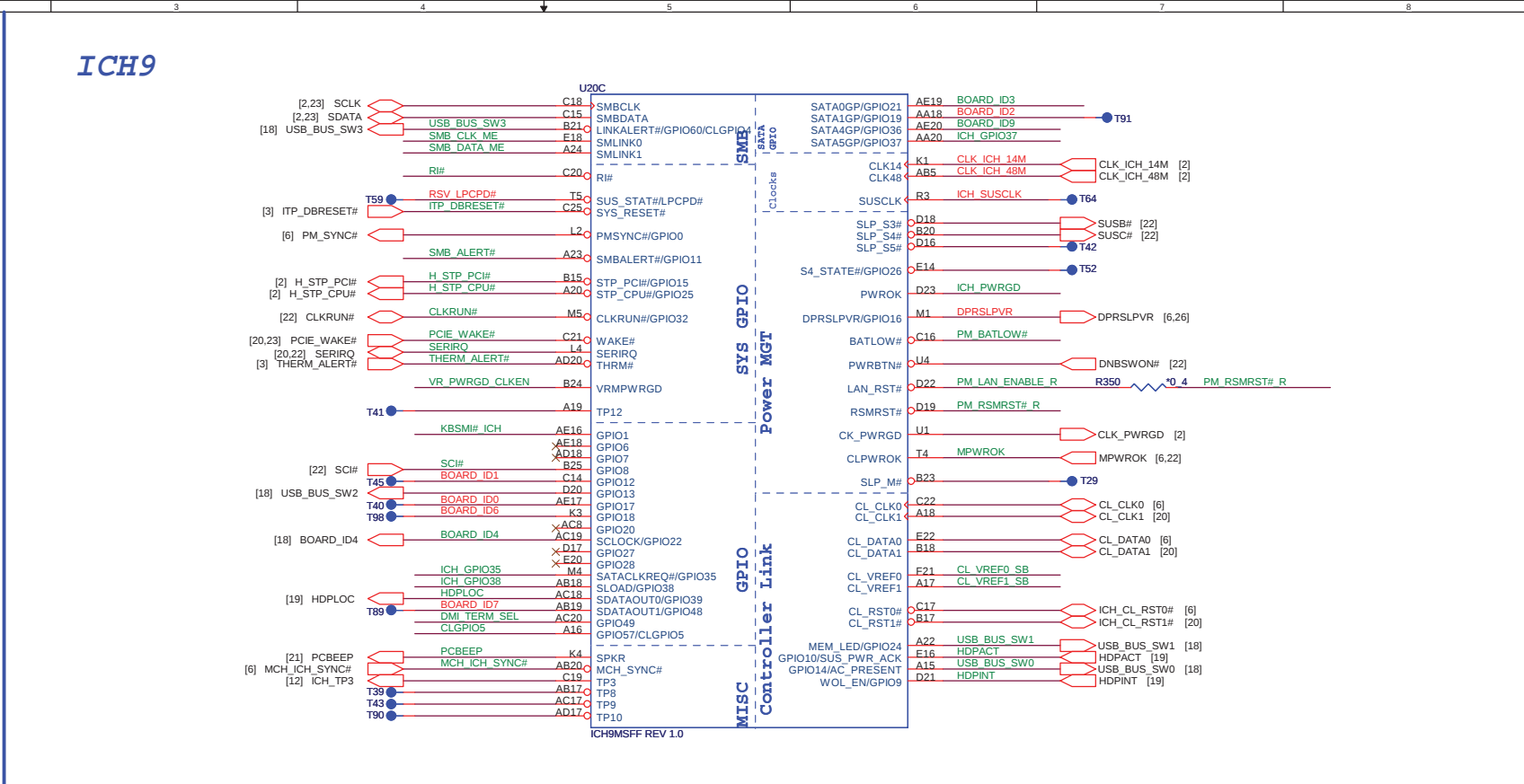


USBOC# PULL-UP



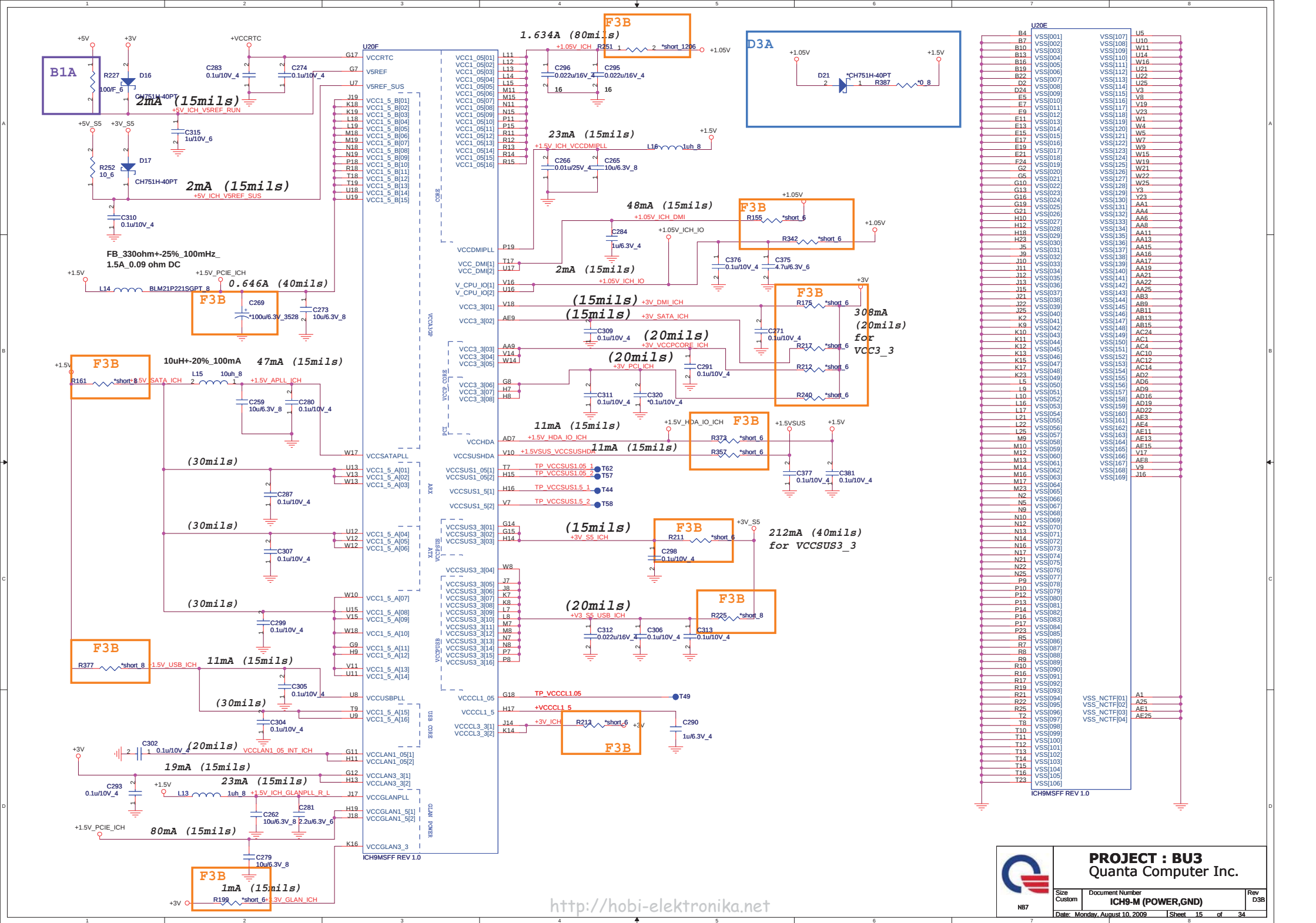
PROJECT : BU3
Quanta Computer Inc.

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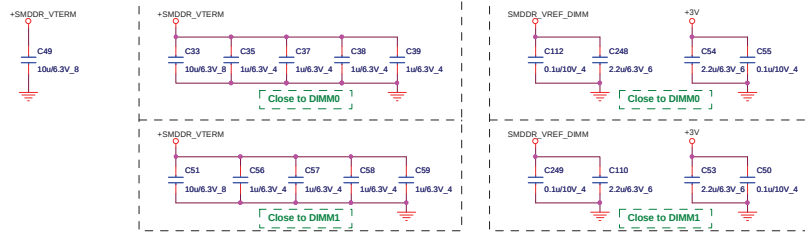


Board ID	ID9	ID4	CPUSB#	ID3
W/ G-SENSOR W/O G-SENSOR	H L			
W/ HDMI W/O HDMI		L H		
W/ 3G W/O 3G			H L	
FOR 11" FOR 13"				H L

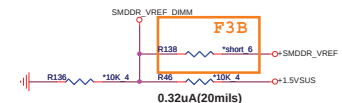
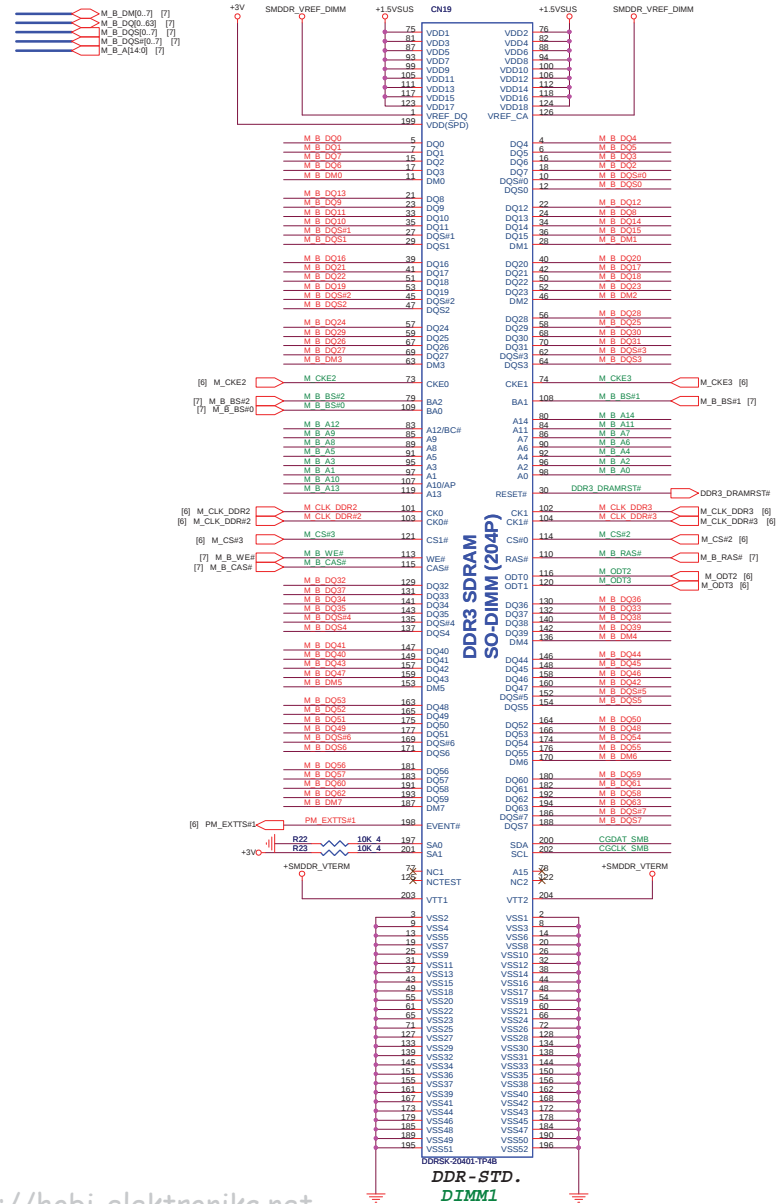
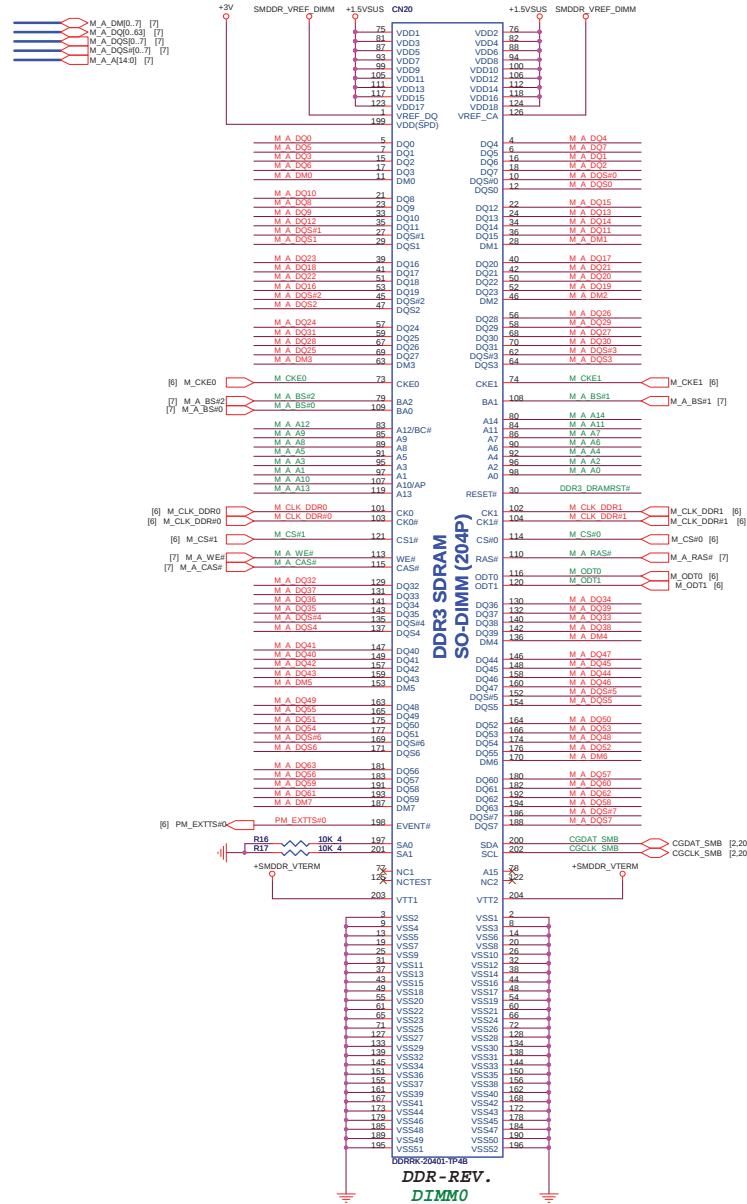
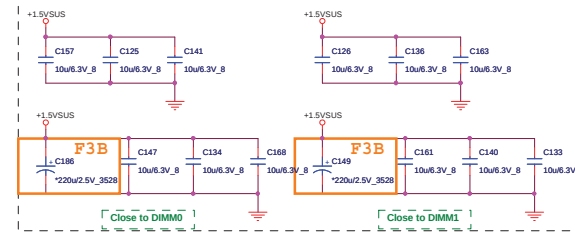
Pin Name	Strap description	Sampled	Configuration	PU/PD
GPIO20	Reserved	PWROK		
PCBEEP	No Reboot	PWROK	0 = Default 1 = No Reboot mode	
GPIO49	DMI Termination Voltage	PWROK	0 = for desktop applications 1 = for mobile applications Internal PU	



TERMINATOR DECOUPLING CAPACITOR

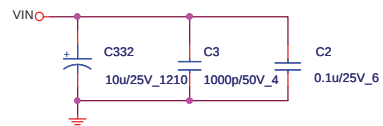


9.12A(VCC plane from source)

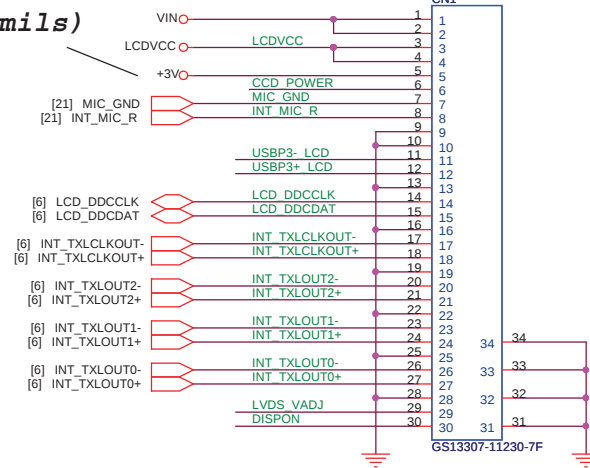


LCD Panel Module

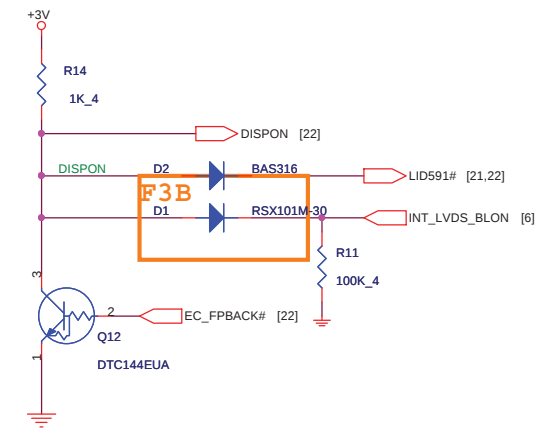
0.3A (20mils)



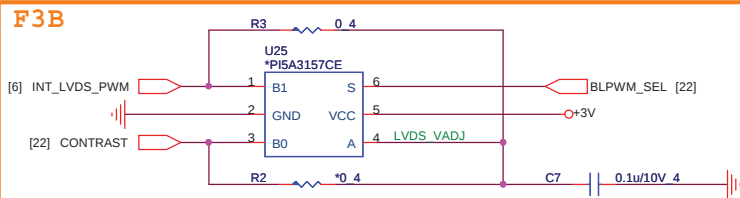
NB Strap
INT_LVDS_EDIDDATA



HALL SENSOR&BACK LIGHT SWITCH

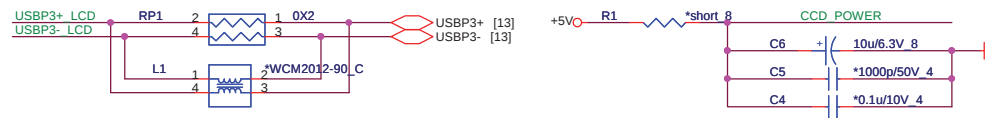


CCD

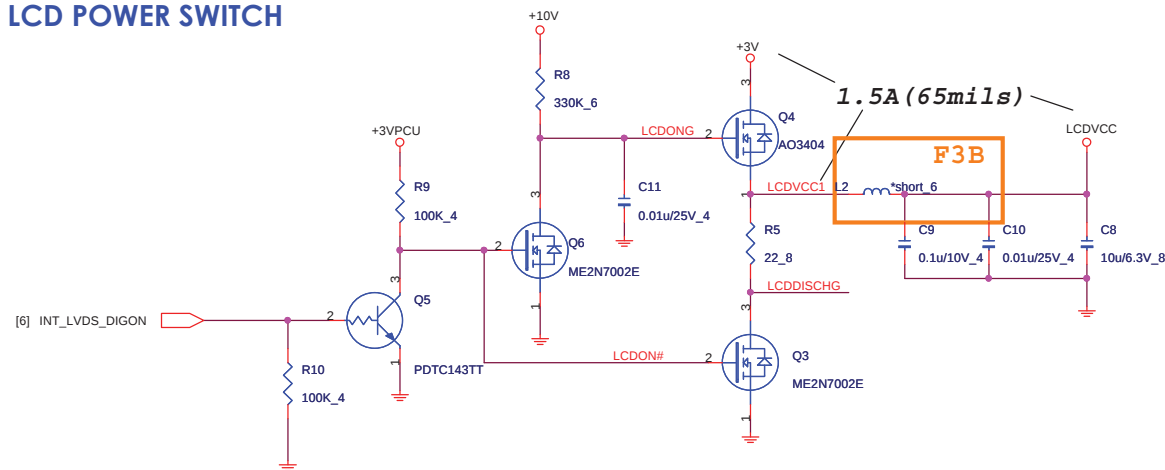


input S	S	S
output A		
INT_LVDS_PWM	H	
CONTRAST		L

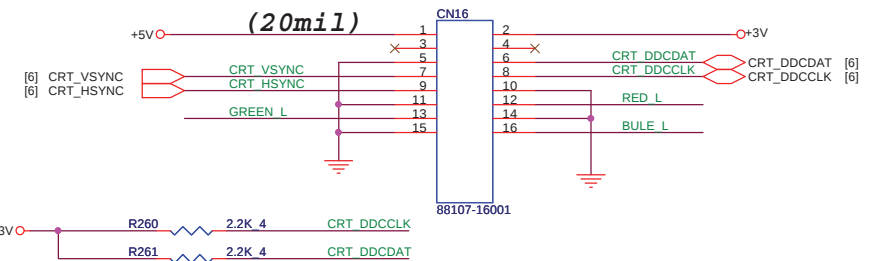
0.2A (20mils)



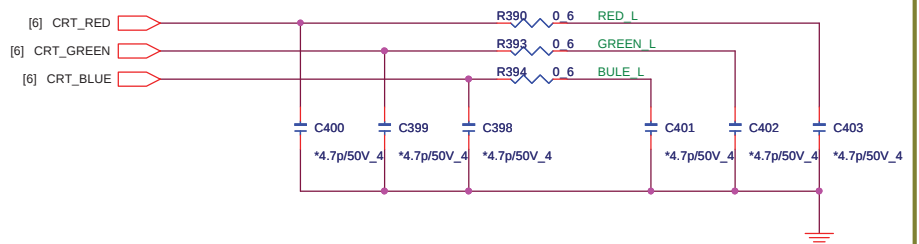
LCD POWER SWITCH



CRT CON.



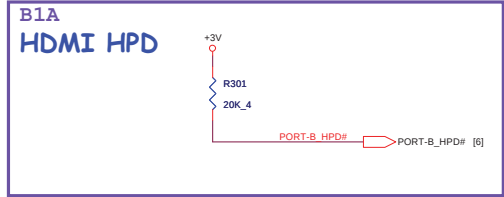
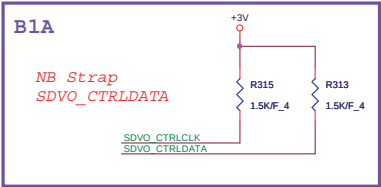
E3A



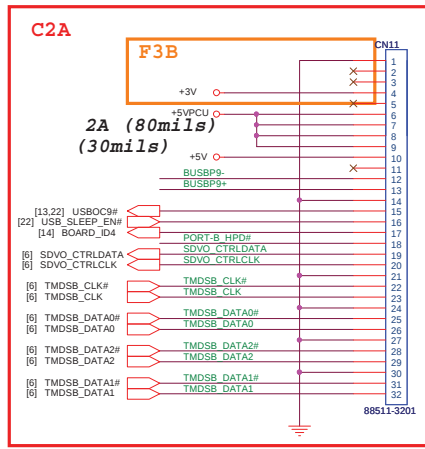
CRT CON. co-lay

E3A

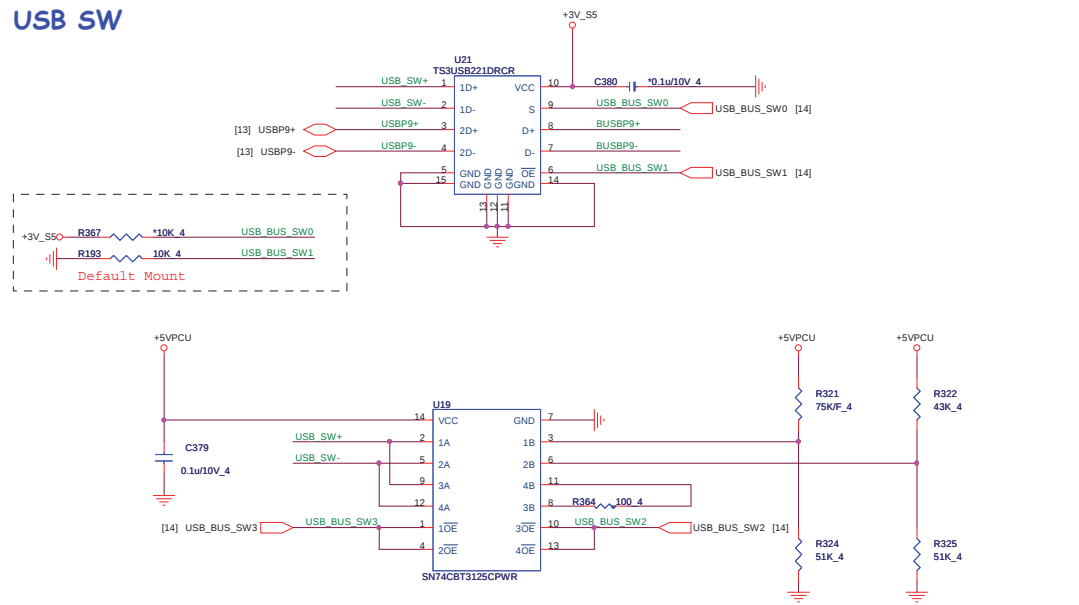
HDMI IC



HDMI CON.



USB SW



EMI

S	OE#	Function
X	H	Disconnect
L	L	D=1D
H	L	D=2D

OE#	Function
H	Disconnect
L	A port= B port

OE#	1OE#	2OE#	3OE#	4OE#
Mode3	High	High	Low	Low
Mode4	Low	Low	High	High

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PROJECT : BU3

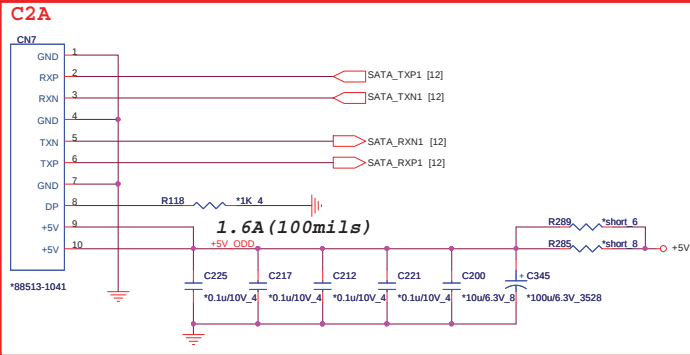
Size Document Number

HDMI/USB SW/EMI

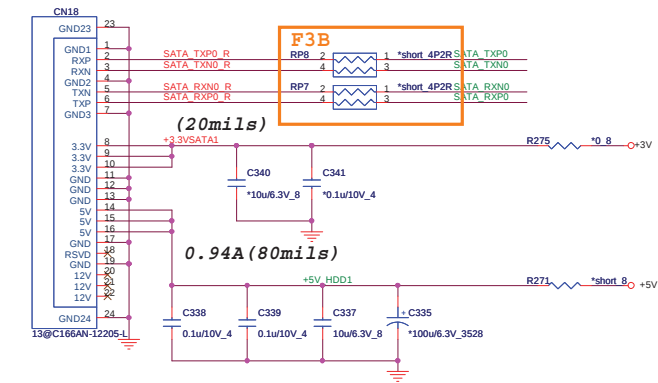
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Rev D3B

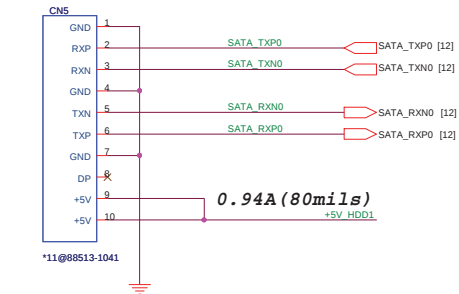
SATA ODD



Main SATA HDD

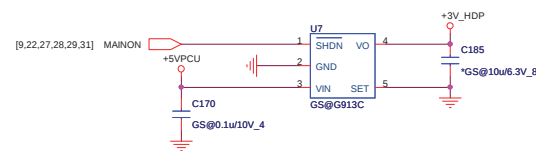


Main SATA HDD (For 11.6")



CO-LAYOUT With MAIN SATA HDD

G-sensor



FS (Full Scale) selection

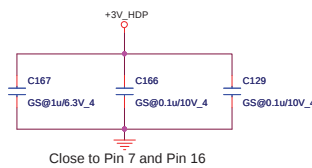
FS	0	1
2g Full-Scale		6g Full-Scale

PD (Power Down) selection

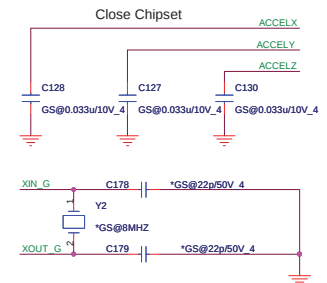
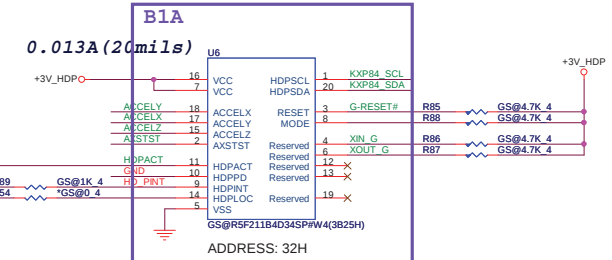
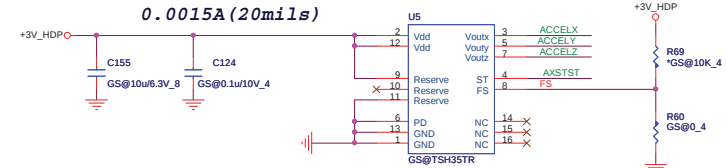
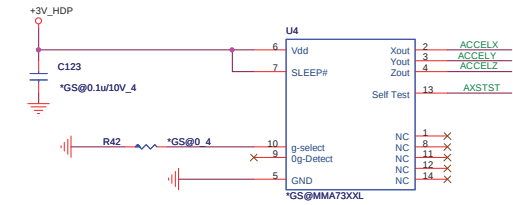
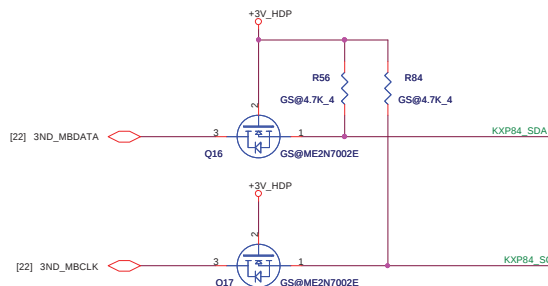
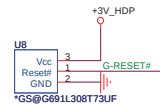
PD	0	1
Normal Mode		Power-down mode

HDPPD selection

HDPPD	0	1
Normal Mode		Power-down mode



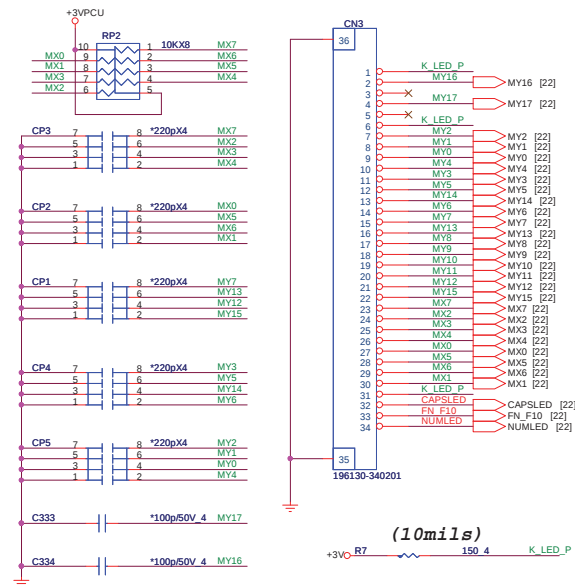
Close to Pin 7 and Pin 16



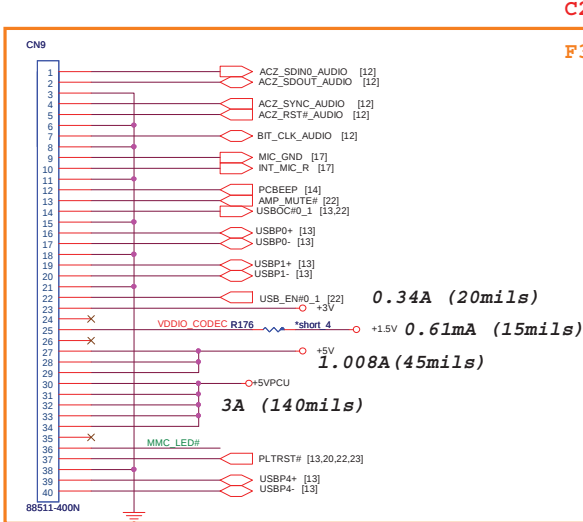
Quanta Computer Inc.
PROJECT : BU3

Size Document Number HDD/ODD/G-sensor Rev D3B
Date: Monday, August 10, 2009 Sheet 19 of 34

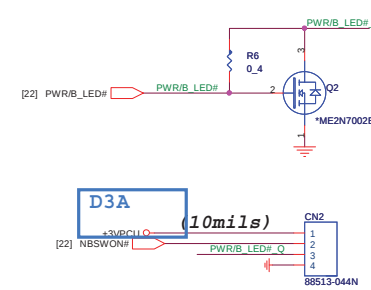
INT Keyboard



USB&FPC&CARDERAD CONNECTOR

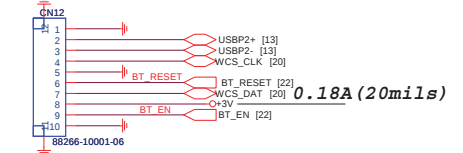


Power board

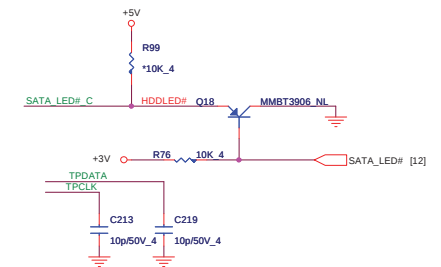
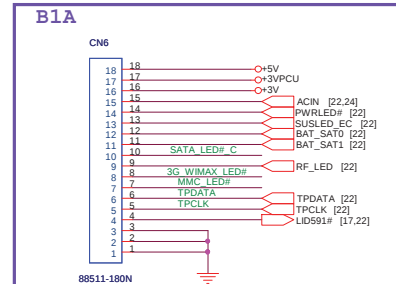


B1A

Bluetooth

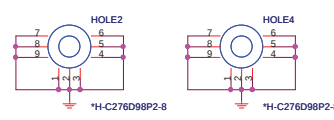
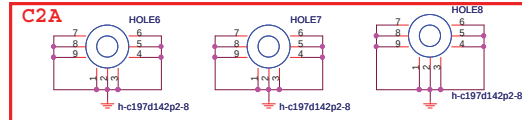


LED/TP/Hall Sensor Con.

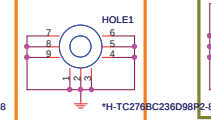


HOLE

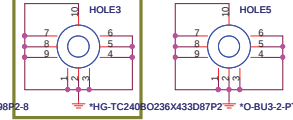
CPU FAN



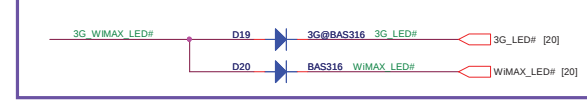
F3B



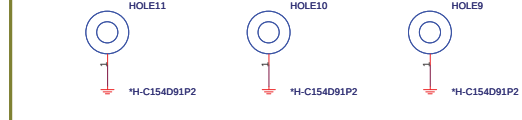
E3A



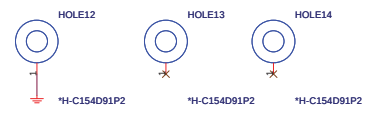
B1A



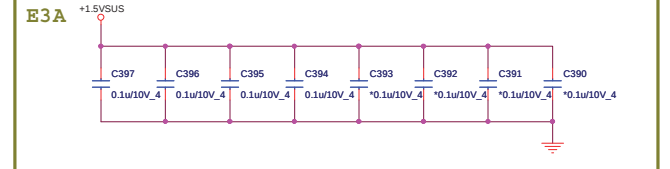
E3A

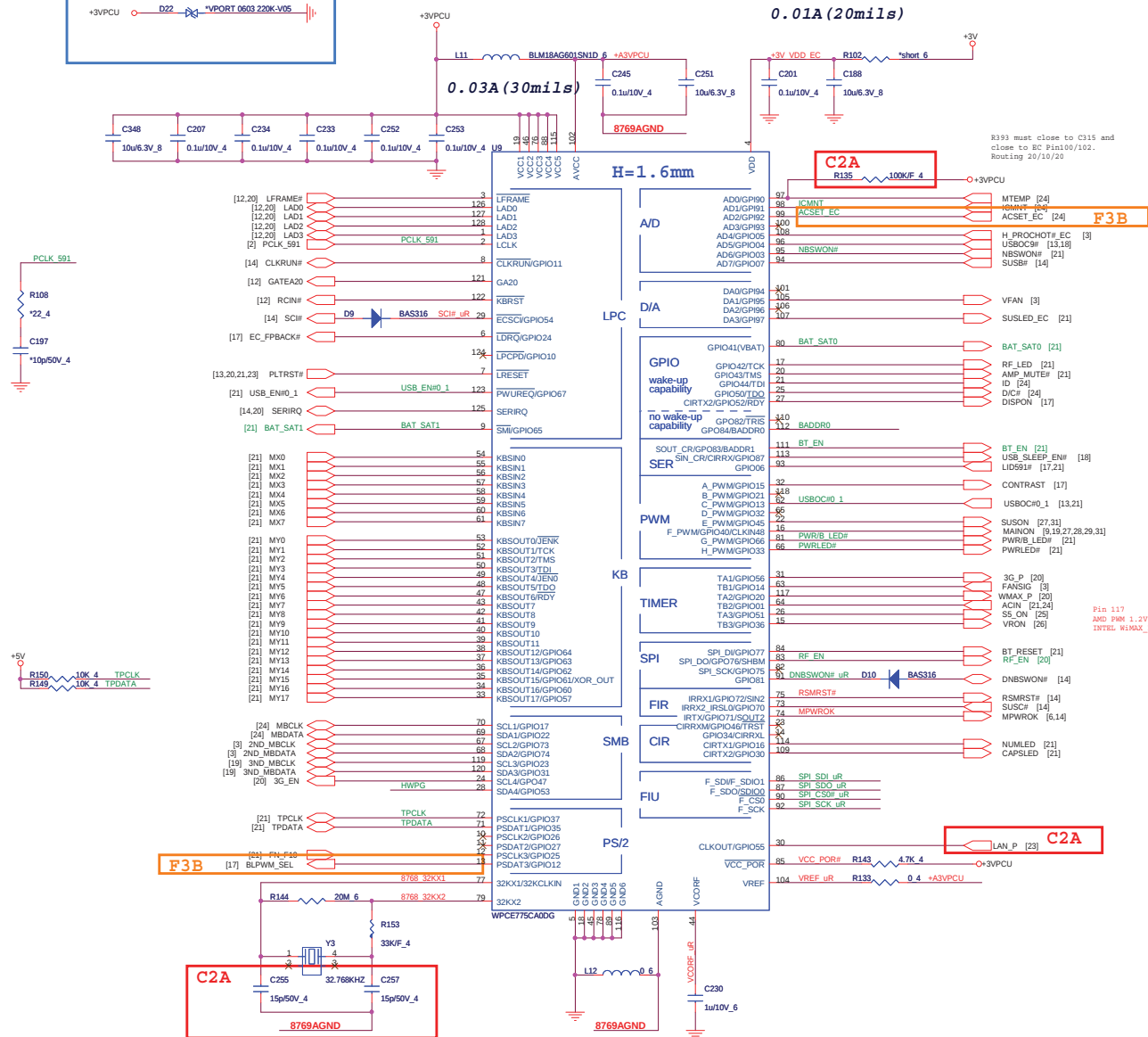


F3B



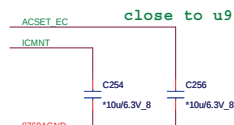
EMI





SMBUS Table

SMBUS	Devices	Address
1	Battery	
2	CPU Thermal Sensor1	98H
	EC EEPROM	A0H
3	3D Sensor	40H

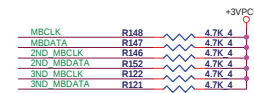


0.01A (20mils)

0.03A (30mils)

R393 must close to C315 and close to EC Pin100/102.
Routing 20/16/20

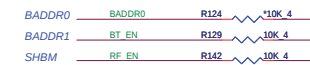
SM BUS PU



I/O Base Address

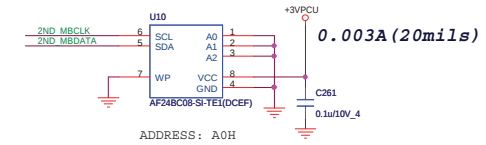
I/O Address		
BADDR1-0	Index	Data
0 0	XOR TREE TEST MODE	
0 1	CORE DEFINED	
1 0	2Eh	2Fh
1 1	164Eh	164Fh

SHBM=0: Enable shared memory with host BIOS

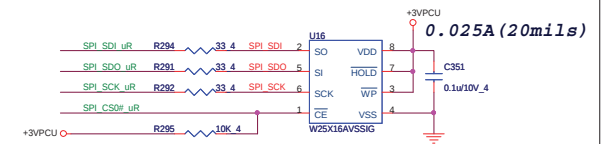


Disabled (*) if using FW device on LPC.
Enabled (V) if using SPI flash for both system BIOS and EC firmware

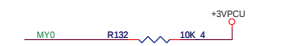
ID



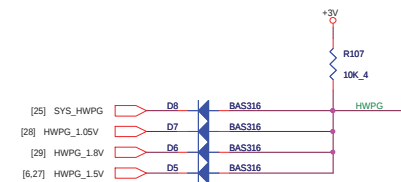
SPI FLASH



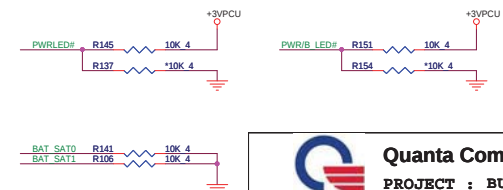
INTERNAL KEYBOARD STRIP SET



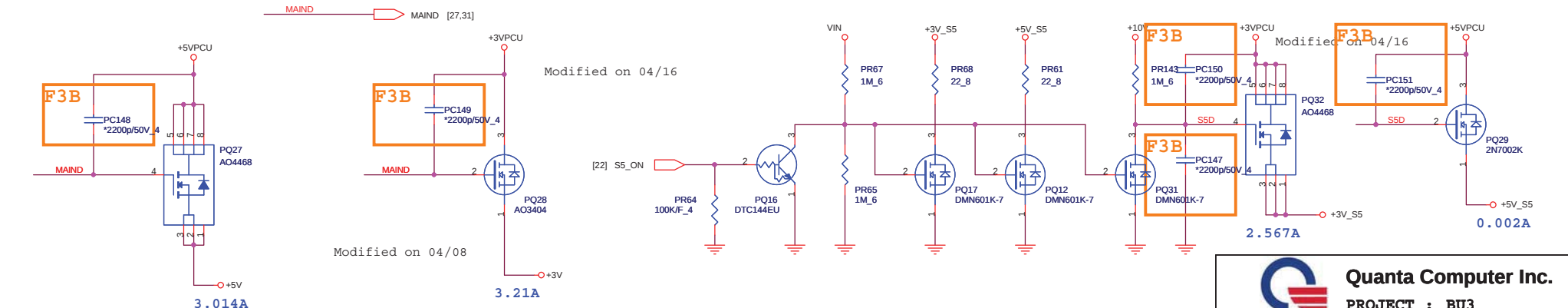
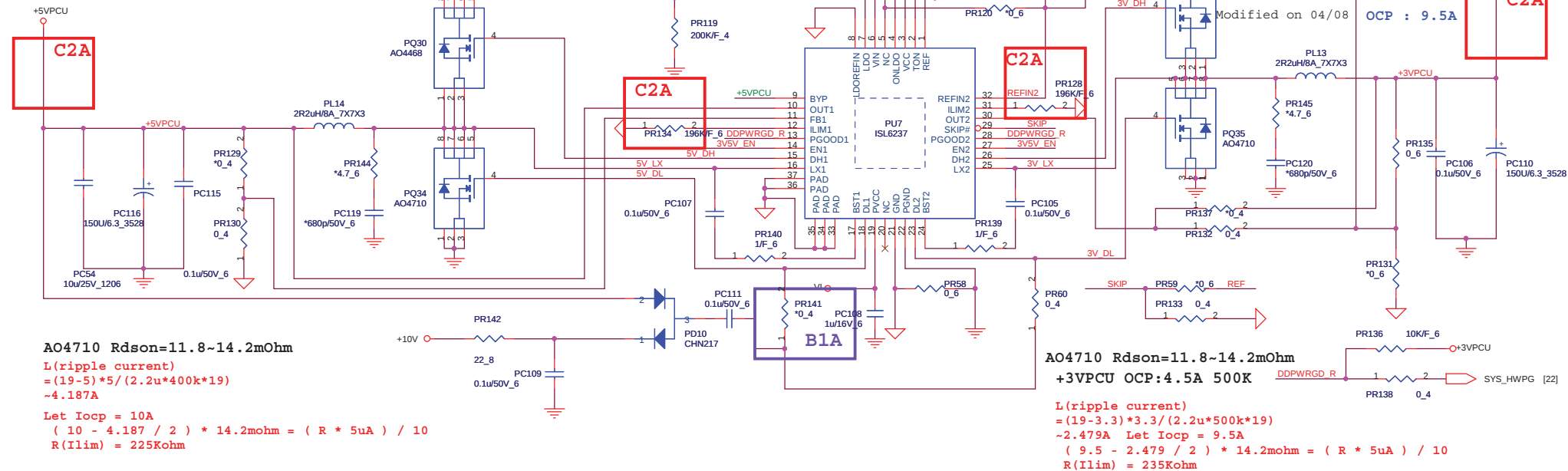
HWPG

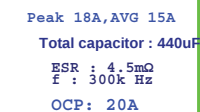


LED

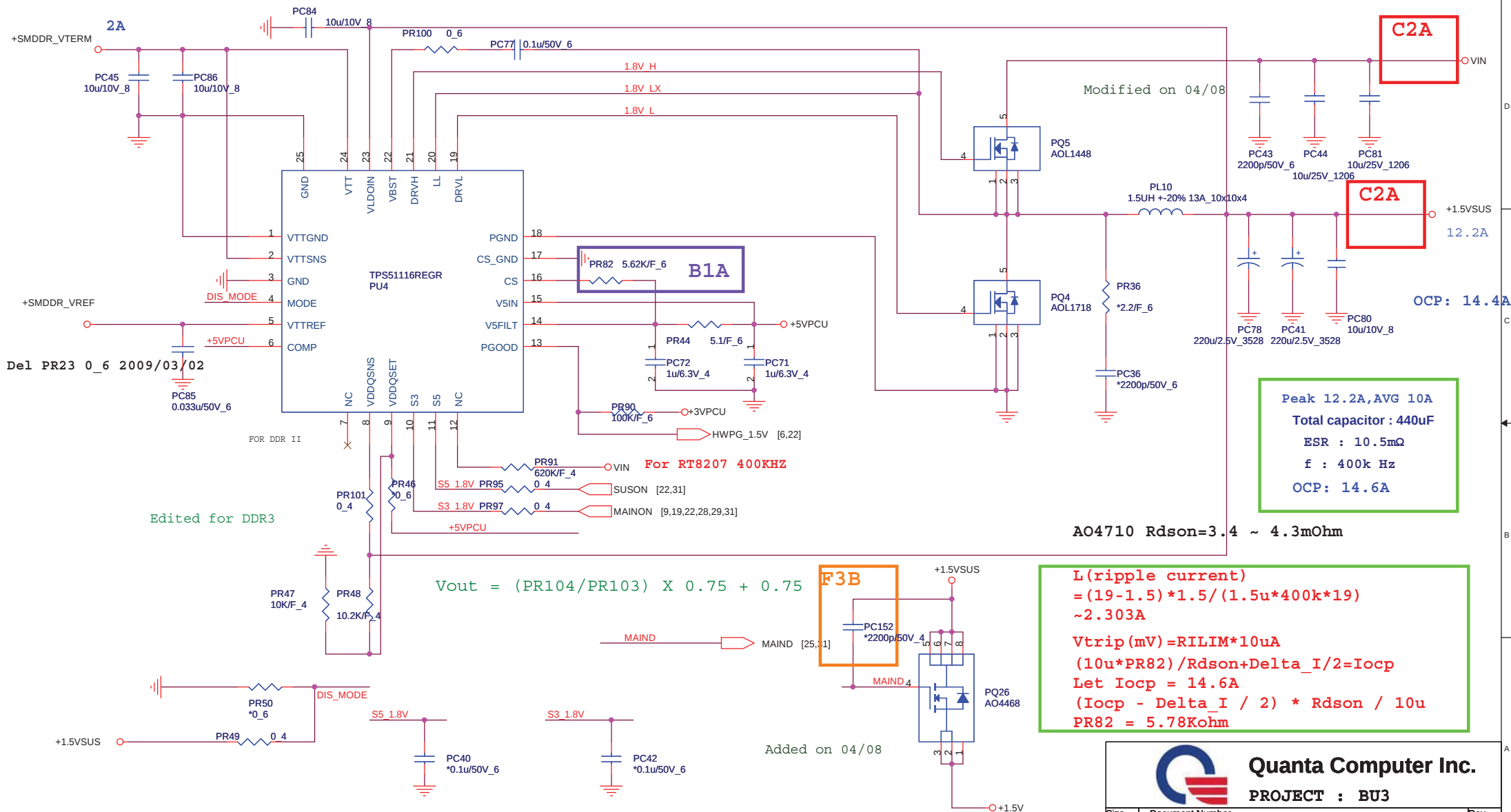


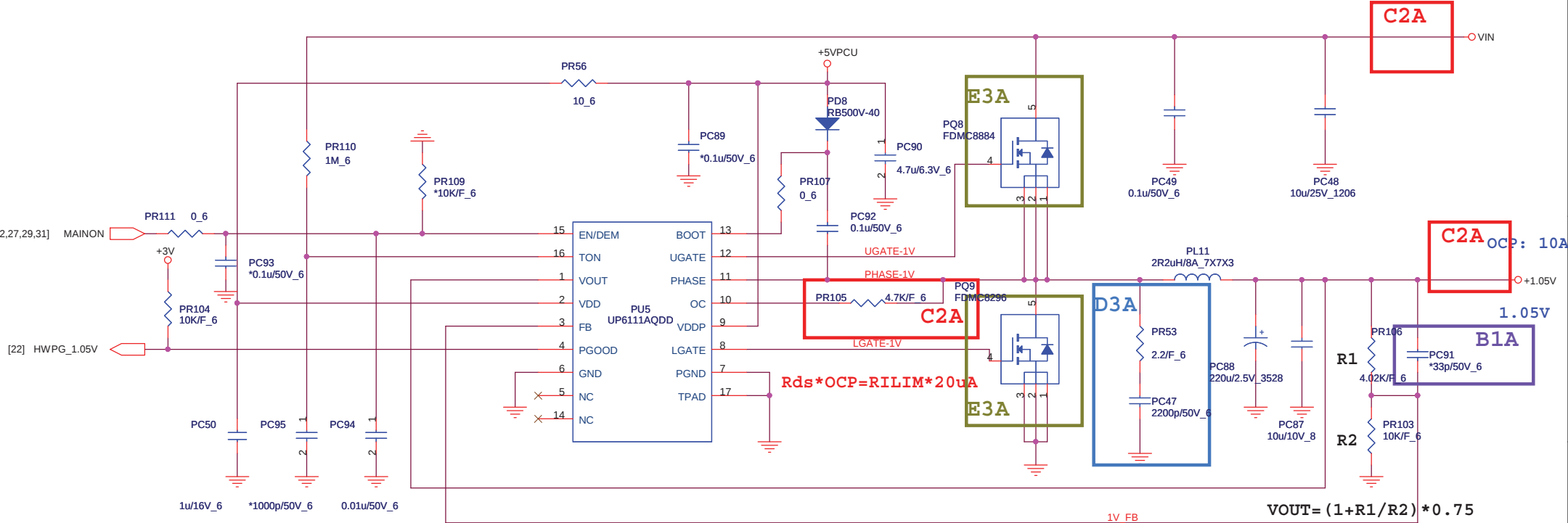
Peak 8.521A,AVG 6.391A
Total capacitor : 160uF
ESR : 25mΩ
f : 400k Hz
OCP: 10A





```
Rocset = ( Ioc * Rdroop) / 10uA
Rdroop = 4mV/A
Ioc = Rocset * 10uA / Rdroop = 20.15A
```





$TON = 3.85p * RTON * Vout / (Vin - 0.5)$
 $TOFF = (Vin / Vout - 1) * Ton$
 $TON = 2.185 * 10^{-7}$
 $TOFF = 3.736 * 10^{-6}$
 $Frequency = 1 / (Ton + Toff) \sim 253K$

FDMC8296 Rdson = 8 mOhm

$L(\text{ripple current})$
 $= (19 - 1.05) * 1.05 / (2.2u * 253k * 19)$
 $\sim 1.78A$

$Let I_{ocp} = 10A$
 $I_{ocp} - I_{ripple} / 2 = RILIM * 20u / Rdson$
 $10 - 1.78 / 2 = RILIM * 20u / 8mohm$
 $RILIM = 3.644Kohm$

(Peak 21.199A, AVG 8A)
 Total capacitor : 230 uF
 ESR : 21mΩ
 f : 253k Hz
 OCP : 10A

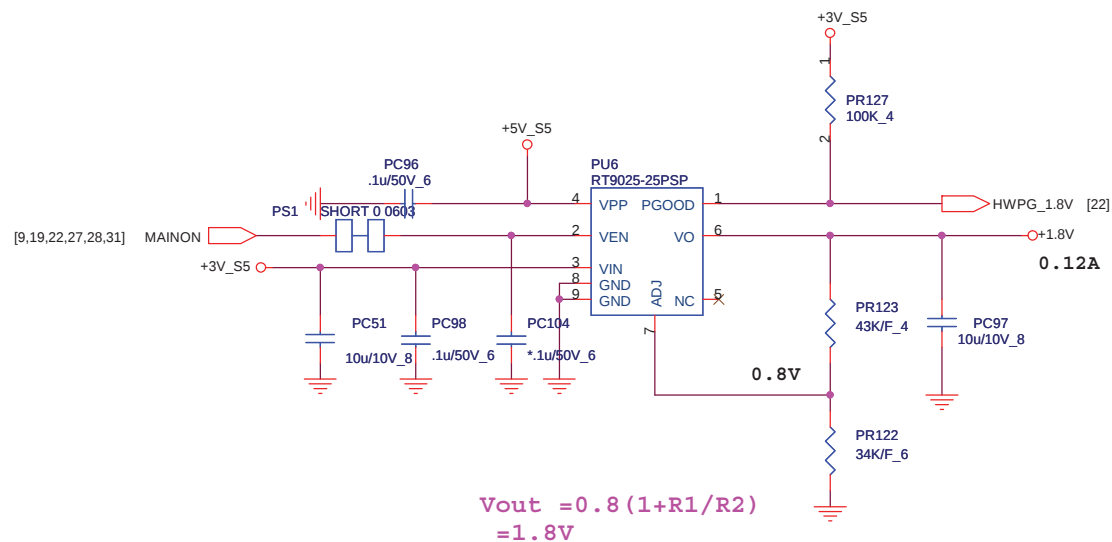


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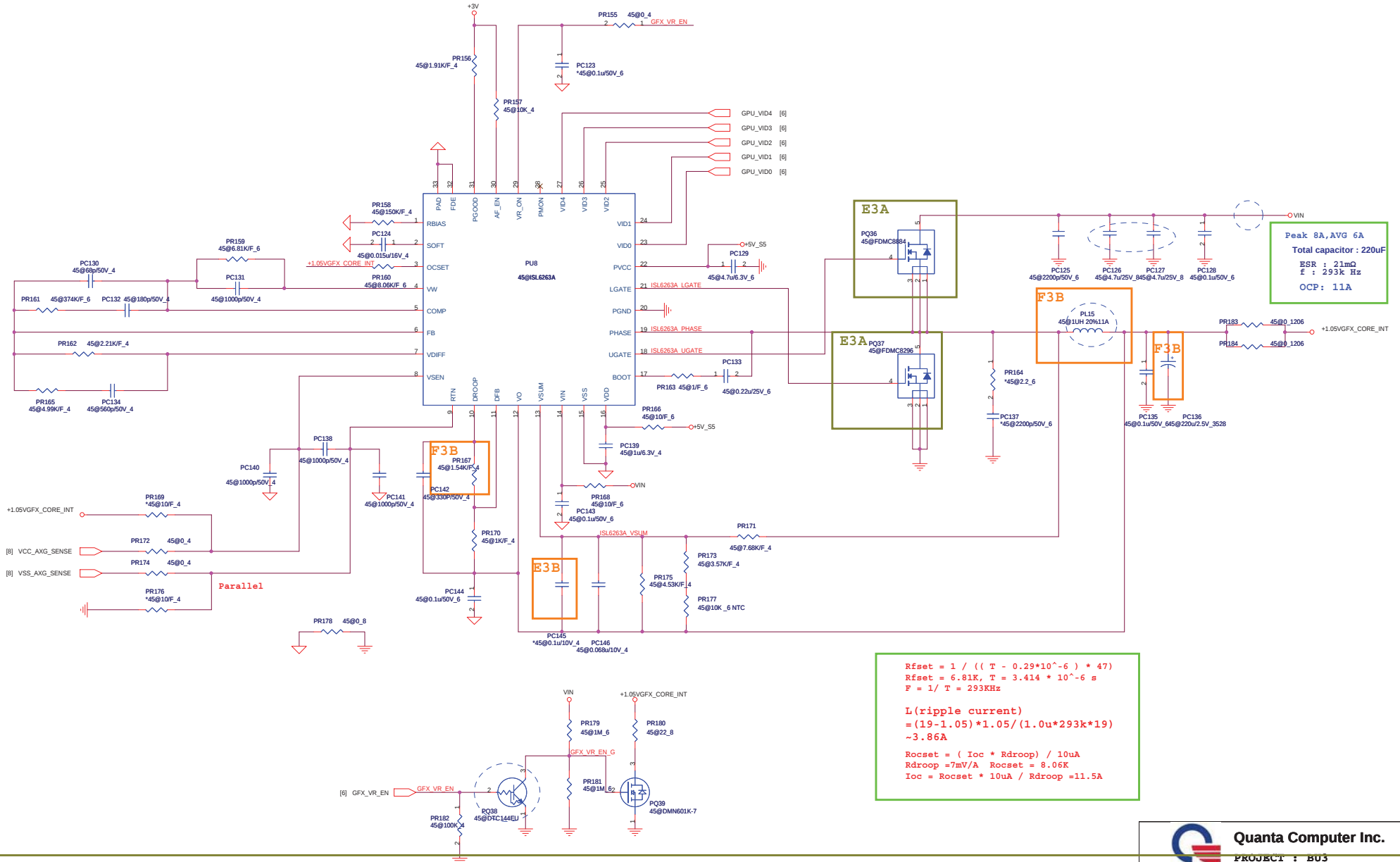
PROJECT : BU3

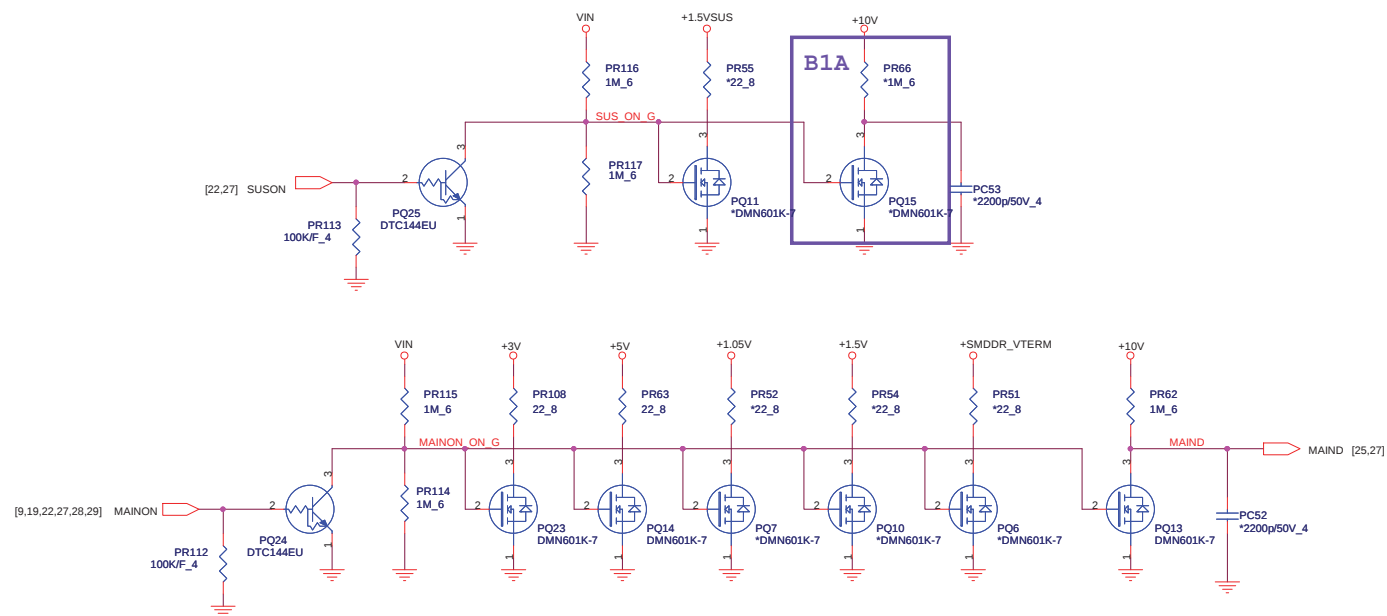
Size	Document Number	Rev
	VCCP 1.05V(UP6111AQDD)	D3B

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E3A

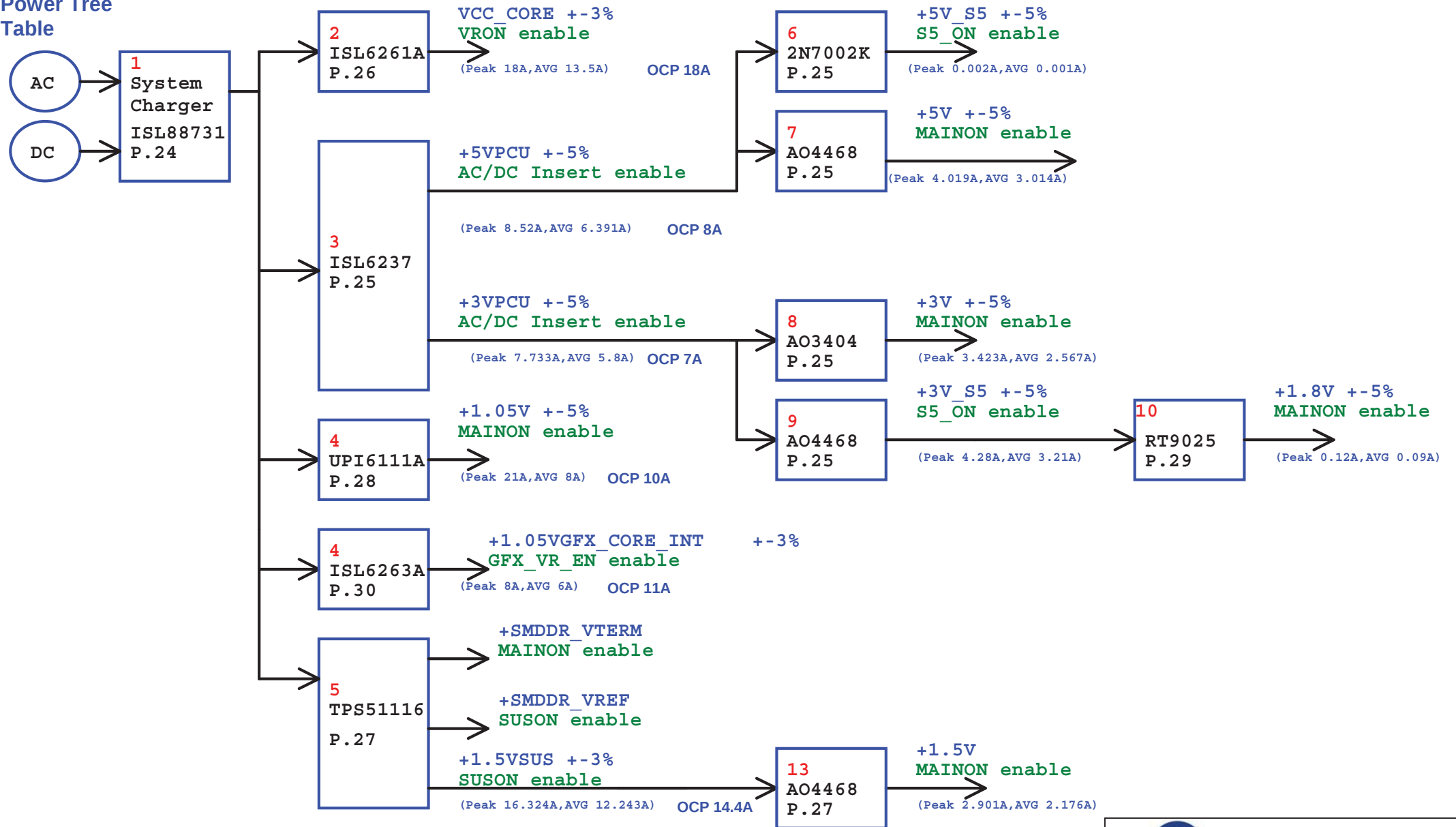




Model		REV	CHANGE LIST		MODEL		BU3	
					PAGE	FROM	To	
BU3 MB	B1B	PAGE 2: add RP21 value 3G@0X2 ,add net name CLK_PCIE_3G to 3G Card pin13 & CLK_PCIE_3G# to 3G Card pin11			1	1A	1B	
		PAGE 13: Add net name PCIE_RXN3,PCIE_RXP3,PCIE_TXN3,PCIE_TXP3 to 3G connector			2	1A	1B	
		PAGE 13: Add C386,C382 both value 3G@0.1u/10V_4			3	1A	1B	
		PAGE 13: del USB5-,USB5+ net			4	1A	1B	
		PAGE 13: add USB7-,USB7+ net to sim connector			5	1A	1B	
		PAGE 18: del HDMI function U17,R298,R299,R303,R305,R307,R309,R320,R323,R308,R306,R304,R310,R319,R317,R302,R297,R296,R312,R157			6	1A	1B	
		PAGE 18: del HDMI function C365,C369,C356,C354,Q28,RN,4,RN5,RNN6,RN3,L20.L21.L22.L23,Q28			7	1A	1B	
		PAGE 20: change Q20 PIN 2 net neme +3V_S5 to WIMAX_P			8	1A	1B	
		PAGE 20: change Q22,Q27 PIN 1 net neme +3V_S5 to +3VPCU			9	1A	1B	
		PAGE 20: Add R380 value 0_8 between net +1.5V and net +1.5V_3G.			10	1A	1B	
		PAGE 20: Add C383 value 0.01V/25_4,C384 value 0.1/10V_4,C385 value 10u/3.6V_8 between net +1.5V_3G and GND			11	1A	1B	
		PAGE 20: change R253,R250 power source +3V_S5 to +3VPCU			12	1A	1B	
		PAGE 20: Connect CN21 PIN 48,PIN 28,PIN 6 to +1.5V_3G			13	1A	1B	
		PAGE 20: Add CN23 value 3G@88266-10001-06 for co-lay SIM card			14	1A	1B	
		PAGE 20: CN21 Connect PIN 33 to PCIE_TXP3,Connect PIN 31 to PCIE_TXN3,Connect PIN 25 to RCIE_RXP3,Connect PIN 23 to PCIE_RXN3			15	1A	1B	
		PAGE 20: Add Q31 value 3G@ME2N7002E,R296 value 3G@10K_4 for PCIE_WAKE to CN21 PIN 1			16	1A	1B	
		PAGE 18: Change CN11 pin define to PORT-B_HPD#			17	1A	1B	
		PAGE 21: Change CN6 footprint and pin define			18	1A	1B	
		PAGE 2: Change CLOCK_GEN_SRC6 net CLK_PCIE_3G and CLK_PCIE_3G# for 3G card			19	1A	1B	
		PAGE 2: Change CLOCK_GEN_SRC4 net CLK_PCIE_MINI1 and CLK_PCIE_MINI1# for mini card 1			20	1A	1B	
		PAGE 20: Change D15 to R297 value 0805 ohm			21	1A	1B	
		PAGE 21: Remove CN13			22	1A	1B	
		PAGE 7: Change R116 value to 12.1K ohm, Add U17 for DDR3_POWER_OK			23	1A	1B	
		PAGE 25: Change PR134 value to 169K ohm, change PR128 value to 174K phm . NC PR141			24	1A	1B	
		PAGE 26: Change PR25 value to 8.06k ohm ,change PR20 value to 1.5K ohm ,change PR4 value to 3.09K ohm ,change PR7 value to 3.24k ohm.			25	1A	1B	
		PAGE 27: Change PR82 value to 5.9k ohm			26	1A	1B	
		PAGE 27: Change PR105 value 9.31K ohm , NC PC91			27	1A	1B	
		PAGE 27: NC PR66,PQ15			28	1A	1B	
		PAGE 20: Change CN22 footprint to minipci-80019-1021-52p-ruv-v ,chabge CN23 footprint to minipci-80052-1021-52p-ldv-v			29	1A	1B	
		PAGE 21: Change HOLE 4 module			30	1A	1B	
PAGE 6: Change R116 value 12.1K/F_4 , add R378 & U22 for DDR3_POWER_OK								
PAGE 6: Change CN6 pin define.								
PAGE 27: Change PR82 value to 5.62K ohm								
PAGE 2: Swap vertical RP11,RP21								
PAGE 15: Change R227 value to 100/F_6								
PAGE 19: Change U6 value to GS@R5F211B4D31SP#W4(0217H)								
PAGE 14: Add R382 to +3V_S5 for ICHP SCI#								
PAGE 17: Change T79,T80,T82,T84,T83,T86, footprint to TP3050								
PAGE 20: Add D19,D20 for 3G_LED# & WiMAX_LED# between CN6 PIN 8 3G_WIMAX_LED#								
PAGE 21: Change CN9 PIN 33 DEFINE for MMC_LED#,change CN6 footprint 18pin								
PAGE 22: Add R135 for battery state issue.								
C2A	PAGE 23: Add Q33 Q32 C388 R383 R384 for LAN_P soft start, change CN4 pin define.							
	PAGE 20: change CN21 CN22 footprint							
	PAGE 20: remove CN13 and change CN8 connector module							
	PAGE 14: R191 always pull high for HDMI & USB BOI-FUNCTION							
	PAGE 18: Change CN11 PIN11 net to BOARD_ID4							
	PAGE 28: remove PL5 ,remove JP3, short by trace.							
	PAGE 27: remove PL4 ,remove JP2&JP1 , short by trace.							
	PAGE 25: remove PL12 &PL15,remove JP5 & JP4, short by trace.							
	PAGE 24: remove PL3 ,short by trace.							
	PAGE 26: PC8 change to CH3474K1B04 CAP CHIP 0.047U 25V(+/-10% X7R 0402)							
	PAGE 21: Change CN9 PIN 24 net to 1.5V							
	PAGE 22: Add R135 for battery leakage current							
D3A	PAGE 26: Add PU1 PIN8 & PIN9 PC121,PC122 CAP CHIP 220P 50V(+/-10%,X7R,0402) to GND SINGAL							
	PAGE 9: Add C389 value 10u/6.3V_8, and change C187 value to 22u/6.3V_8 for CRT power noise issue,(reserve U23)							
	PAGE 24: Change PU3 Part number to AL088731001							
	PAGE 22: Change C255 and C257 value to 15p/50V_4							
	PAGE 14: Change R156 Part Number to CS23243F930							
	PAGE 12: Add R385 ,R386 for USB-ODD CO-LAY.(reserve)							
	PAGE 24: Change PD4 Footprint to d-5_375-3_975 for OPEN issue							
	PAGE 21: Change CN2 PIN1 NET from +5VPCU to +3VPCU							
	PAGE 20: Change R379 value to 100K_4 for WIFI INTEL module issue							
	PAGE 13: Add R388,R389 for reserve gemalto 3G sim card							
	PAGE 18: Reserve D21 and R387 to keep voltage 0.4 V							
	DOC NO. 204		PROJECT MODEL :	BU3	APPROVED BY:	Mosy Li	DATE:	2009/04/27
PART NUMBER:			31BU3MB0000	DRAWING BY:	Mosy Li	REVISION:	1B	
								Quanta Computer Inc. PROJECT : BU3

Model		REV	CHANGE LIST				MODEL			BU3		
							PAGE	FROM	To			
BU3 MB	D3A	PAGE 26: Add PR146,PR147,PR148 value 0_4 ,PR149 value 10K/F_4 for power suggest				1	1A	1B				
		PAGE 22: Add D22 for ESD/EOS suggestion - Power pin EOS				2	1A	1B				
		PAGE 22: C386,C382,RP21不上件				3	1A	1B				
		PAGE 02: change C373,C374 value to 33p/50V_4 for XTAL report				4	1A	1B				
		PAGE 20: reserve Q31,R381,R380,C383,C384,C385				5	1A	1B				
	E3A	PAGE 17: reserve CRT FILTER R390,R393,R394,C398,C399,C400,C401,C402,C403 for EMI requirement.				6	1A	1B				
		PAGE 21: add C390,C391,C392,C393,C394,C395,C396,C397 for EMI requirement .				7	1A	1B				
		PAGE 30: add 1.05v GFX SCHEMATIC for reader stand by function (GS45 only)				8	1A	1B				
		PAGE 28: change PQ8 and PQ9 value and footprint .				9	1A	1B				
		PAGE 17: Add R3,R2 BOI-OPTION for GS40.				10	1A	1B				
	F3A	PAGE 17: Add R392 ,R391 for Board ID3				11	1A	1B				
		PAGE 21: Add HOLE 9,HOLE 11, HOLE 10.				12	1A	1B				
		PAGE (12) :Change R244 to bead 120ohm, C324 to 22PF for EMI requirement.				13	1A	1B				
		PAGE (24) : Add PR88, PR35 for Adapter Voltage monitor				14	1A	1B				
		PAGE (17) : Reserve U25 for LVDS_VADJ option (support XP function key).				15	1A	1B				
		PAGE (25) : Reserve PC147,PC148,PC149,PC150,PC151,PC152 for power soft start				16	1A	1B				
		PAGE (21) : Change CN9 connector pin define to 40 pin				17	1A	1B				
		PAGE (17) : Change D1 footprint				18	1A	1B				
		PAGE (18) : Change HDMI CN11 connector PIN DEFINE				19	1A	1B				
		PAGE (22) : R176,RP7,RP8,L2,R138,R161,R377,R199,R251,R351,R213,R225,R211,R373,R357,R240,R212,R217,R175,R342,R155,R48,R59,R112,R111,R130,R131,R288,R284,R62,R91,R41,R134 replace by short pad				20	1A	1B				
		PAGE (22) : R378,R68,R279,R12,RP17,RP15,RP16,RP14,RP13,RP12,RP11,RP10,RP9,R293,R8 replace by short pad				21	1A	1B				
		PAGE (22) : Change CN9 pin define. 40PINS				22	1A	1B				
		PAGE (30) : Change PL15 from 2.2uH to 1uH , PC145 change to unmounted , PR167 change to 1.54K , PC136 should be mounted for 3D hang up issue.				23	1A	1B				
		PAGE (09) : reserve C186,C149,C269,C247,C113,C342,C154,C135 for cost down				24	1A	1B				
						25	1A	1B				
						26	1A	1B				
						27	1A	1B				
						28	1A	1B				
						29	1A	1B				
						30	1A	1B				
DOC NO. 204		PROJECT MODEL :	BU3	APPROVED BY:	Mosy Li	DATE:	2009/04/27	Quanta Computer Inc. PROJECT : BU3 Change list Size Document Number Date: Monday, August 10, 2009 Sheet 32 of 33 Rev 038				
		PART NUMBER:	31BU3MB0000	DRAWING BY:	Mosy Li	REVISION:	1B					

Power Tree Table



Quanta Computer Inc.
PROJECT : BU3

Size	Document Number	Rev
		D3B
Power Tree Table		
Date:	Monday, August 10, 2009	Sheet 34 of 34